Cost-Effective High-Performance Flip Chip *Micro*LeadFrame® (fcMLF®) Package Introduction

Luke Hoefer, KyungSu Kim
Amkor Technology Inc.
2045 E. Innovation Circle
Tempe, AZ 85249 USA

Abstract

The demand for cost-effective leadframe packages continues to grow, particularly for automotive and commercial applications. These designs require smaller form factors, enhanced thermal and electrical performance, and proven reliability. Flip chip on leadframe technology offers significant advantages over traditional wire-bonded *Micro*LeadFrame® (MLF®) and high-cost laminate Flip Chip Chip Scale Package (fcCSP) designs, including enhanced thermal and electrical characteristics and reduced package size compared to traditional wirebond solutions such as MLF®. As industry standards push for cost effective solutions targeting thinner and more compact profiles than available in wirebond solutions, flip chip technology enables die size reduction and printed circuit board (PCB) area savings compared to conventional wire-bonded MLF® packages. The use of copper (Cu) pillar bumps supports fine-pitch designs and offers flexibility for fan-in leadframe configurations. The flip chip *Micro*LeadFrame (fcMLF®) package presents a compelling solution for a wide range of applications, including power management integrated circuits (PMICs), DC/DC converters, and RF switches. As with a traditional MLF® package, Amkor's wettable flank feature, both dimple and step-cut configurations can be supported. A requirement of the automotive industry, the wettable flank enhancement enables Automated Optical Inspection (AOI) for proper fillet formation during the Printed Circuit Board (PCB) solder reflow process without requiring an expensive and complex through board X-Rays process. By leveraging industry-leading flip chip interconnect technology and an established sawn MLF® manufacturing process, fcMLF® packaging delivers a cost-effective, high-performance leadframe packaging solution tailored to meet the evolving needs of modern electronic systems.

Keywords

Cost Effective, Copper Pillar, fcMLF®, Side Wettable Flank, Size Reduction, Thermal Efficiency

I. Introduction

The relentless march of semiconductor scaling continues to reshape the packaging landscape, driven by Moore's Law and the demand for higher performance in increasingly compact form factors [1]. Over the past two decades transistor density has increased exponentially, with leading-edge processes now achieving densities exceeding 100 million transistors per square millimeter.

Certain applications such as RF and PMIC devices have evolved alongside advanced-node components, creating a codependent ecosystem operating under high frequency and increased current density conditions. In these mixed environments, high-performance devices generate significant heat, placing new thermal demands on adjacent legacy packages such as wirebond MLF® (QFN). As a result, MLF® designs available today are faced with two critical challenges: improved electrical performance and enhanced thermal dissipation.

While the wirebond MLF® technology may have limitations, advanced flip-chip solutions offer a way to overcome many of the electrical challenges. Optimizations to signal path geometries and the minimization of parasitic elements may be accomplished with a flip-chip tailored die and leadframe design, which has the potential to improve device performance. However, it is important to note that flip chip designed products such as Flip Chip Ball Grid Array (FCBGA), fcCSP, and fcMLF® solutions often require advanced materials and processes which will impact the overall cost of the package and assembly processes.

A typical fcMLF® package utilizes copper pillar bumping for the die to package interconnects, enabling shorter electrical signal paths that enhance device level performance.

Achieving these benefits depends on fine pitch leadframe design flexibility, which is critical for meeting the performance demands often required by a fcMLF® device. If necessary, a copper Re-Distributed Layer (RDL) can be utilized to achieve the bump pitch requirements of fan-in type leadframes. It is important to note that the RDL may impact the device level performance and will certainly impact the assembly cost. fcMLF® packages also offer wettable flank designs allowing for high speed Automated Optical Inspection (AOI) of the solder fillet when the package is mounted on the board. Finally, the characteristic MLF design consisting of a heat sink mounted below the die is carried over into fcMLF, allowing for efficient thermal dissipation even in high power density applications.

With its enhanced signal path geometry, robust thermal dissipation, and compatibility with established wirebond MLF lines, fcMLF® is a compelling solution for PMICs, DC/DC converters, and RF devices. Supporting a range of power and signal capabilities, fcMLF bridges the gap between traditional MLF and advanced flip chip packages, delivering high-end capabilities in a compact, cost-effective format.

II. Electrical Performance

Electromagnetic Interference (EMI) is of particular concern in high frequency and high power applications. Generated by a combination of factors including impedance mismatch and parasitics, these electromagnetic emissions can result in logic errors and device malfunctions in sensitive peripheral nodes. Allowable levels of EMI are outlined in various international and regulatory standards such as CISPR (International Special Committee on Radio Interference) and FCC Part 15 guidelines [2, 3]. With the ever-increasing signal speeds of Integrated Circuits (ICs) and an increasing density of components for enabling compact application systems, EMI and signal integrity issues have been elevated to greater importance [4]. As a result, flip-chip packaging solutions such as fcMLF® have emerged as critical enablers for modern packaging and system design.

One of the key factors in mitigating EMI is by ensuring a resonance-free system, which is generally achieved by first identifying and then matching impedance along the I/O interconnect pathway [5]. Package impedance can be characterized using an electrical circuit model consisting of resistive, inductive, and capacitive elements (RLC). RLC simulations were performed in conjunction with various types of packages to better understand their exhibited electrical performance. As shown in Figure 1, simulation results revealed that fcMLF® devices significantly outperformed MLF® and fcCSP packages while nearly matching WLCSP package impedance at frequencies of 500 MHz and 1 GHz. Capacitive reactance was assumed negligible due to the common practice of adding matching capacitors on the final product, allowing the analysis to focus on the impact of package inductance on overall impedance.

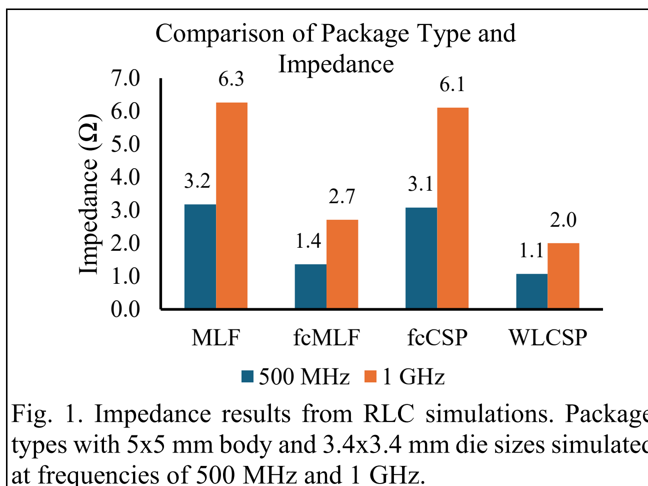

Fig. 1. Impedance results from RLC simulations. Package types with 5x5 mm body and 3.4x3.4 mm die sizes simulated at frequencies of 500 MHz and 1 GHz.

The difference between 1 Ω and 6 Ω of impedance makes little difference in the package characteristics, as decoupling or matching capacitors will be required to minimize noise and match trace impedance regardless. However, increasing frequency does increase impedance, and while operation at 1 GHz may not surpass impedance criteria higher frequency operation certainly will if package design is not taken into consideration. This is where fcMLF® excels, with simulated impedances 2.3x less than that of wirebond MLF® devices. Lower impedance gives the designer greater flexibility in PCB layout for peripheral components that are often needed to achieve application signal level matching requirements. As such, the capability of the fcMLF® package to efficiently suppress electromagnetic emmisions and maintain signal integrity while operating at high frequencies represents a significant advantage [6]. These advantages are especially valuable in RF applications, where the short signal paths of fcMLF® can deliver superior signal integrity and enable significant device level differentiation in competitive markets. Further, fcMLF® also has potential in PMIC applications as successful impedance matching reduces potential voltage drops or spikes, which is essential to reduce stress on the power delivery network (PDN) and ensure stable operation [7].

In addition to EMI emissions catalyzed by impedance mismatch, parasitic inductance is a critical factor influencing both EMI and signal integrity. Arising from inductive elements within a package, parasitics typically manifest in the form of bond wires, vias, and traces – which can distort signal waveforms during fast switching events. At high

frequencies, even small inductive values can lead to substantial voltage spikes. These spikes contribute to overshoot and undershoot, which results in signal ringing and degrades signal fidelity. This may also radiate EMI into periphery nodes. Traditional wirebond packages are particularly susceptible to parasitic inductance due to their longer and more variable interconnect paths, while advanced packages such as fcCSP and WLCSP are prone to parasitic inductance due to longer substrate signal traces. These interconnect paths can be visualized in Figures 2 and 3.

Fig. 2. Step cut wirebond MLF® cross sectional view. Wires extend from the die pads to the leadframe with loop geometry.

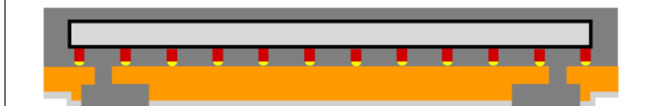

Fig. 3. Step cut fcMLF® cross sectional view. Copper pillar bumps extend from the die directly into the leadframe, reducing interconnect path length.

As previously depicted in the simulated package impedances shown in Figure 1, fcMLF® outperforms wirebond MLF® and fcCSP packages with inductances of 0.4nH. In relation to capacitance, fcMLF® packages were in line with MLF® and outpaced fcCSP and WLCSP as seen in Figure 4.

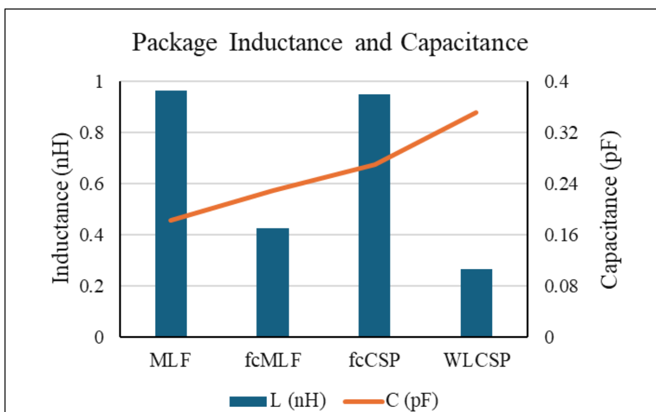

Fig. 4. Inductance and Capacitance simulated for various package types with 5x5 mm body and 3.4x3.4 mm die sizes.

Package inductance and impedance optimization collectively enhance signal integrity, suppress high-frequency emissions, and support reliable operation in high-speed, high-power environments. For this reason, fcMLF® packaging stands as a robust electrical solution with potential performance advantages over other package solutions.

III. Thermal Performance

As die level power densities continue to rise, effective package level power dissipation becomes a critical factor in ensuring reliability and performance. Power dissipation considerations are further advanced by the growing pressure for package size reduction, which concentrates thermal energy. The leadframe based structure of fcMLF® is well suited to meet the growing challenges in heat dissipation, as unlike traditional wbMLF® the fcMLF® configuration boasts thermal enhancement availability on the top and bottom of the die. The traditional wirebond MLF® package utilizes an exposed die attach pad, a feature well recognized on the bottom side of most MLF® (QFN) packages. This feature may be implemented in fcMLF® designs or left out due to package size and/or design limitations. The exposed die attach pad can be seen in Fig. 5.

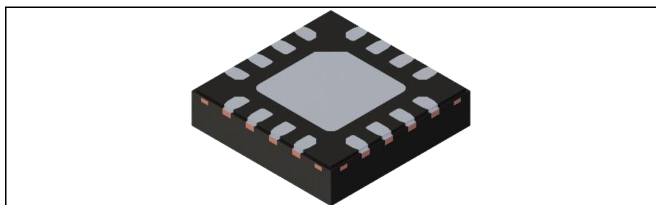

Fig. 5. Step cut fcMLF® with bottom leads and heat sink facing up. Wirebond MLF® package has an identical bottom configuration, only in a larger package.

In fcMLF®, the exposed pad supports multiple die level thermal vias attached directly to the pad, thus enabling improved thermal dissipation into the PCB through PCB ground plane interconnects. Thermal diffusion away from the die can be represented by three terms, Θja, Θjb, and Θjc. Θja is representative of junction-to-ambient thermal resistance and is a predictor of overall heat dissipation, with lower values indicating better dissipation.

Thermal modeling was performed between wirebond MLF®, fcMLF®, fcCSP, and WLCSP devices to better understand thermal dissipation and resistance characteristics. Results reveal that fcMLF® devices closely match the Θja of wirebond MLF® devices (33.6 vs. 36.1 °C/W) as shown in Table I and are significantly better at dissipating thermal energy than WLCSP or fcCSP devices.

PKG Type	Body (mm)	Die (mm)	Θja (°C/W)	Θjb (°C/W)	Θjc (°C/W)
MLF®	5x5	3.4x3.4	33.6	13.5	1.89
fcMLF®	5x5	3.4x3.4	36.1	6.4	1.04
fcCSP	5x5	3.4x3.4	50.1	20.7	0.11
WLCSP	3.4x3.4	3.4x3.4	51.2	30.6	13.2

Table I. Various package types are compared by body size, die size, and heat dissipation.

Θjb, or junction-to-board thermal resistance, is significantly lower for fcMLF® packages, indicating a significant improvement in board-level thermal performance. Compared to wirebond MLF® and fcCSP/WLCSP designs, fcMLF® exhibits approximately 2 to 5x lower thermal resistance, respectively. This reduction in Θjb translates to a smaller temperature increase under equivalent power dissipation.

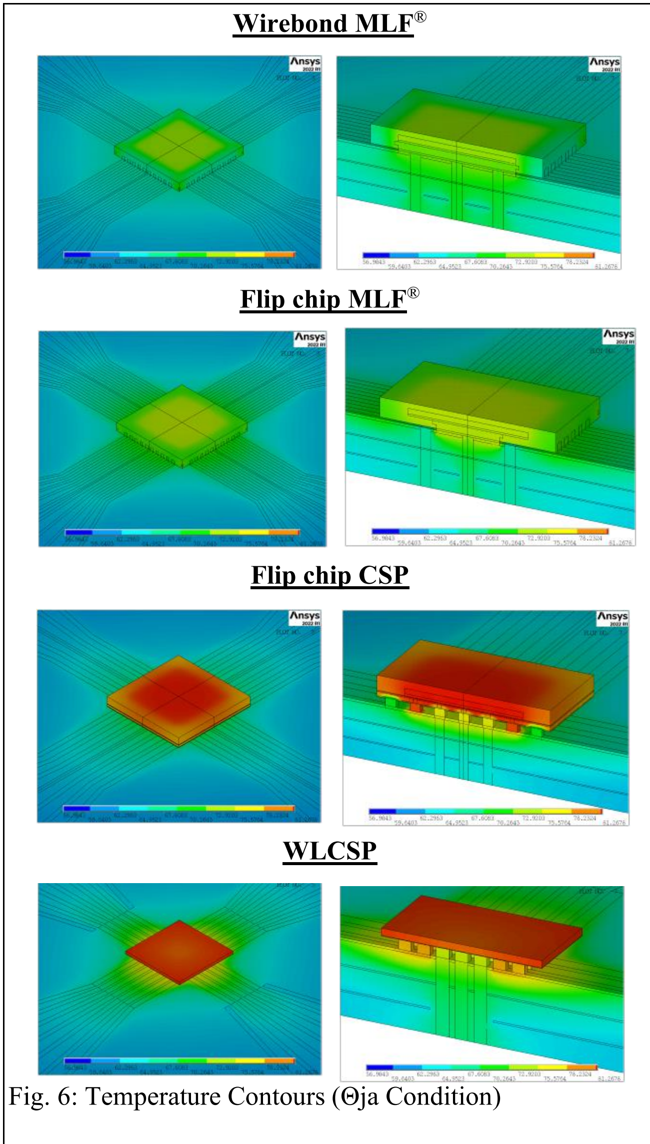

Fig. 6: Temperature Contours (Θja Condition)

This enhanced thermal efficiency positions the fcMLF® packaging solution to be particularly well-suited for power applications where board-level heat dissipation is critical. Thermal imaging of the total model isotherm and an additional cross section view can be seen for the various package considerations in Figure 6.

The simulation results demonstrate that the fcMLF® package exhibits an enhanced thermal performance when compared to traditional wirebond MLF® designs with significant performance improvement compared to the fcCSP and WLCSP alternatives. With Θja values notably lower than fcCSP and WLCSP, the fcMLF® packaging technology ensures efficient board-level heat dissipation. This translates to lower junction temperatures under identical operating conditions, of critical importance for applications with demanding power dissipation requirements.
Combined with its compact footprint and cost-effective manufacturing, fcMLF® offers a compelling solution for applications where thermal efficiency and space optimization are paramount.

IV. Package Characteristics

As semiconductor applications grow increasingly complex, the demand for compact, high-density packaging has intensified. Package dimensions play a critical role in enabling system-level integration and board space optimization. As a leadless packaging technology, the MLF® packaging solutions address these constraints by minimizing package body dimensions, including height. However, wirebond geometry still requires that pads be placed along the periphery and the mold cap be sized to enclose the wire loops, adding to package footprint and height. fcMLF® packaging solutions extend the capabilities of MLF® technology by utilizing die bump to leadframe interconnects as a replacement to the wire bond interconnect pads. Interconnect pads can then be moved below the die, enabling smaller and thinner packaging solutions (See Figure 7).

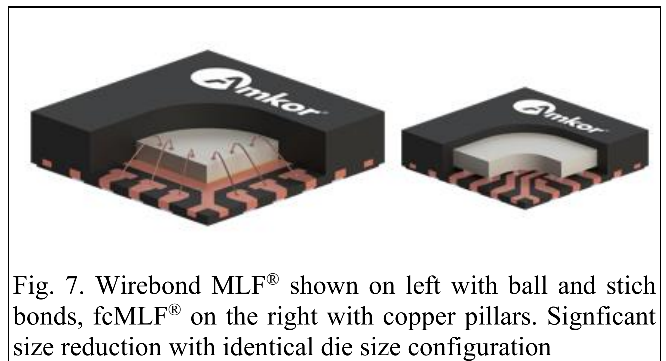
Fig. 7. Wirebond MLF® shown on left with ball and stich bonds, fcMLF® on the right with copper pillars. Signficant size reduction with identical die size configuration

In addition to the package footprint improvements, fcMLF® devices offer greater flexibility in package height due to use of die bumping for interconnect. As a result, the distance between the die top and mold cap can be reduced as much as 100 µm. In certain cases, the height can be reduced further by thinning the die prior to bumping or by modifying the EMC mold cap thickness. By comparison, wirebond MLF® with a wire loop geometry raised above the package requires ≥100 µm of distance between the die top and mold cap for thin dies (≤76 µm thickness). For more traditional wirebond

MLF® packages a die top to mold cap thickness of 350 – 400 µm is common.

Considering a nominal Cu pillar bump height of 80 µm (pre-collapse) and a leadframe thickness of 6 mm combined with a thinner die and mold cap, a fcMLF® solution can significantly reduce the overall package thickness. These features enable the fcMLF® package thickness to be <350 µm. Other techniques can be applied to reduce package profiles even further.

The fcMLF® package, similar to MLF®, supports the wettable flank step cut feature. As denoted by Figure 8, the process exposes a portion of the leadframe sidewall, allowing for visual inspection of the solder joints when mounted on the PCB rather than requiring X-Ray.

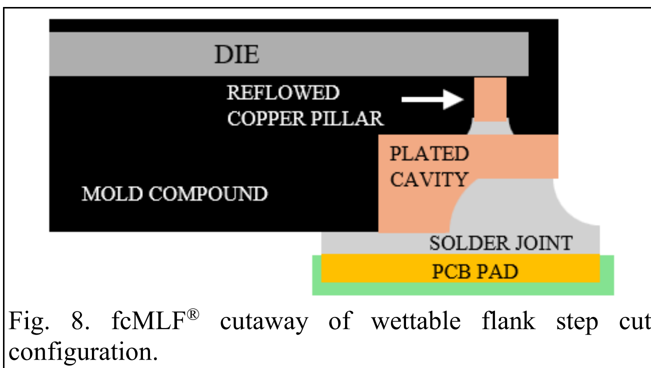

Fig. 8. fcMLF® cutaway of wettable flank step cut configuration.

Due to the fillet formation, Automated Optical Inspection (AOI) is a widely adopted industry practice for verifying proper device attachment to the PCB [8]. The ability for fcMLF® to utilize automated inspection equipment is a significant advantage for PCB assembly. By contrast, FCBGA, fcCSP, and WLCSP all require more complex methods of solder joint inspection such as through board X-Ray. Furthermore, depopulation of components or spacing required to enable effective X-Ray techniques often results in unused areas on the PCB and increases board size.

fcMLF® step cut wettable flank designs are applicable for lead pitch configurations between 0.3-1 mm and a body size of 1-7 mm. These ranges are depicted in Figure 9.

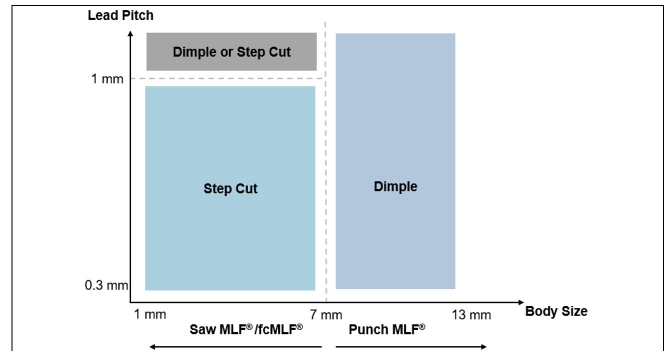

Figure 9: Attributes for wettable flank selection and design.

V. Manufacturing Optimization

MLF® technology is a mature manufacturing process and utilizes a highly optimized manufacturing flow. Its widespread adoption within industry is observed in automotive, consumer, and industrial applications and has cultivated a robust ecosystem of tooling, materials, and process controls. This maturity has been translated into exceptional cost efficiency, reliability, and manufacturing productivity, making it an ideal foundation for next-generation packaging innovations.

By design, the fcMLF® manufacturing process utilizes much of the MLF® established infrastructure with the addition of the die flip chip onto leadframe and reflow processes. This compatibility not only reduces the need for specialized equipment but also enhances overall manufacturing efficiency while accelerating device/product time-to-market.

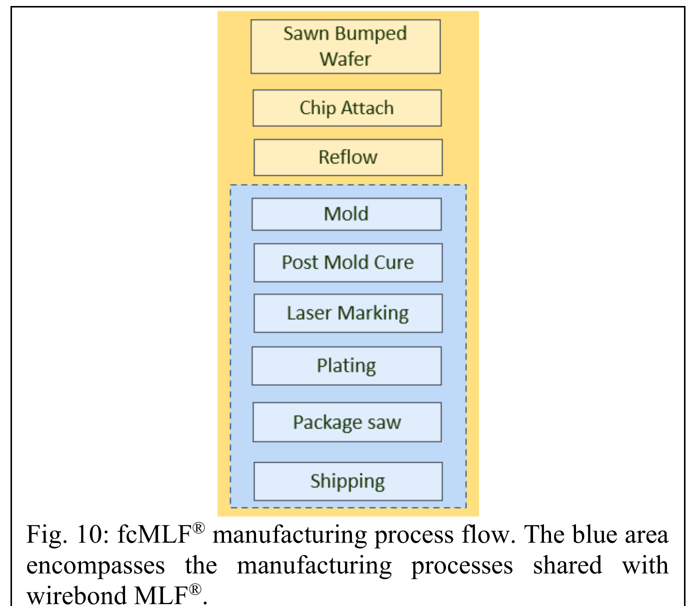

Fig. 10: fcMLF® manufacturing process flow. The blue area encompasses the manufacturing processes shared with wirebond MLF®.

fcMLF® utilizes the same copper leadframe material as the MLF®. This commonality ensures that a supply chain for leadframes is maintained and consistent between the two

technologies. As a result, sourcing concerns are mitigated and cycle time for new design introduction can be reduced. Shorter development time for the new designs can also equate to a reduction in time to market, with the added benefit of possible replacement of fcMLF® devices for wire bond MLF® versions.

VI. Conclusion

As semiconductor applications continue to demand higher performance in increasingly compact and cost-sensitive designs, packaging technologies must evolve to meet these challenges without sacrificing manufacturability. The fcMLF® package stands at the intersection of innovation and practicality by enabling electrical and thermal performance enhancements while maintaining the manufacturing efficiency and scalability of the MLF® leadframe technology.

By leveraging copper pillar flip chip technology, fcMLF® addresses the limitations of traditional wirebond interconnect designs by offering reduced electrical parasitic effects, enhanced signal integrity, and improved thermal dissipation. At the same time, the benefits of the fcMLF® technology compatibility with the mature and highly optimized MLF® manufacturing flow ensure seamless integration into existing high-volume production lines. This shared infrastructure minimizes disruption, enables cost effective manufacturing, and reduces deployment time. Combined, these noted benefits make fcMLF® an ideal robust solution for use in automotive, power management, and RF applications.

References

[1] Moore, G. E. (1965, April 19). *Cramming more components onto integrated circuits*. Electronics, 38(8), 114–117.

[2] International Electrotechnical Commission. (2021). *CISPR 25:2021 – Vehicles, boats and internal combustion engines: Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers* (5th ed.). IEC

[3] Federal Communications Commission. (2025). *47 CFR Part 15 – Radio frequency devices*. Electronic Code of Federal Regulations.

[4] *Development of Sub-mm Wave Flip-Chip Interconnect*, Cuvillier Verlag, 2016. *ProQuest Ebook Central*. Chapter 2.

[5] Olney, B. (2018, Febuary). *Beyond design: The target impedance approach to PDN design.* ICD.

[6] LaMeres, B., & Khatri, S. P. (2010). *Broadband impedance matching for inductive interconnect in VLSI packages*. Montana State University.

[7] Witcher, S., & Sandler, S. (2023). *A New Power Integrity Requirement to Supplement Target Impedance: Quantifying PDN Impedance Flatness*. DesignCon 2023. Picotest.

[8] Mangrum, M. A. (2020). *Side wettable flanks for leadless automotive packaging* [White paper]. Amkor Technology, Inc.