# Readying the supply chain for chiplets and heterogeneous IC packaging

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Products using heterogeneous integration (HI) and chiplets are here, they are in production, and the current trend is for more products and more customers to develop and qualify their products at outsourced semiconductor assembly and test suppliers (OSATs) and foundry providers.

Combinations of processors and memories have been around for years, culminating at the high end with processors and high-bandwidth memory (HBM) to address a fast-growing market for artificial intelligence (AI) algorithm training. Now, the functional de-partitioning of die functions into chiplets is enabling a broader and more potent impact on future designs. Chiplet approaches allow product performance increases to continue at a cost point that is still compelling. Total silicon costs can be lower due to better yields for smaller chiplets, and the opportunity to use a mixture of silicon process nodes to further optimize the cost of the silicon. Integrated circuit (IC) packaging for heterogeneous and chiplet approaches is more expensive, but this rise in package cost is offset by reduced total silicon expenses and favorable time-to-market advantages.

Moving to chiplets and HI implementations has required a new infrastructure to be established for IC and package design, IC and package fabrication, and electrical test. Design tools need to comprehend multiple ICs in 2D and 3D physical configuration, functional device electric test (E-Test) and higher power densities. IC packaging to support chiplets, and heterogeneous constructions, have been a primary focus for OSATs and foundries in recent years. Multi-die products must be integrated into one functional unit. Such integration is accomplished using higher-density integration approaches, namely wafer-scale (chip-on-wafer, CoW) high-density modules and high-density multi-chip modules (MCMs), or both. High-density modules are then attached to the IC package substrate in a production environment like the venerable system-on-chip (SoC) flip-chip ball grid array (FCBGA) packages, but with several key customizations.

Currently, the packaging methodologies employed in both production and development encompass the following: 1) 2.5D through-silicon via (TSV) modules relying on silicon interposers, i.e., 2.5D TSV; 2) modules utilizing high-density fan-out (HDFO) multi-layer redistribution layer (RDL) approaches; or 3) modules featuring bridges. These two-dimensional constructions can be used for discrete die combinations as well as combinations of discrete die and 3D die stacks. The sections below discuss this developing landscape, starting first with the 2.5D TSV.

## 2.5D TSV silicon interposers

2.5D TSV has been in high-volume manufacturing (HVM) at Amkor since 2017. The process flow begins with a full "TSV-reveal" capability, starting with full thickness interposer wafers from one of the foundries, thinning to reveal the Cu TSVs, followed with an inorganic passivation step, under bump metallization (UBM) and interposer backside bumping.

This product space is dominated by high-performance processors working in combination with high-bandwidth DRAM memory (HBM), including HBM2, HBM2e and HBM3. 2.5D TSV was one of the first modern heterogeneous integrations using a high-density module to permit integration of the processor and DRAM in the package itself. The silicon-based interposer uses a Cu backend foundry fabrication process, and this enables 1-2µm lines and spaces inside the IC package. This has been critical to enable a very wide parallel data base for HBM communication. In many ways, it was this process development to enable 2.5D TSV taking place in 2015-2018 that set the stage for a new class of high-density module-based products. These new approaches targeted the next wave of heterogeneous integrations as chiplets that were being designed and qualified in just the last few years. In addition to the latest processing know-how developed to support the TSV reveal process, a new class of ultra small Cu pillar bumps was required to support bump pitches in the 40-55µm range. This requires advanced plating tools and chemistries.

Many of the foundational technologies noted above were used as is or extended to intersect other high-density modules such as HDFO and bridge-based product developments (**Figure 1**).

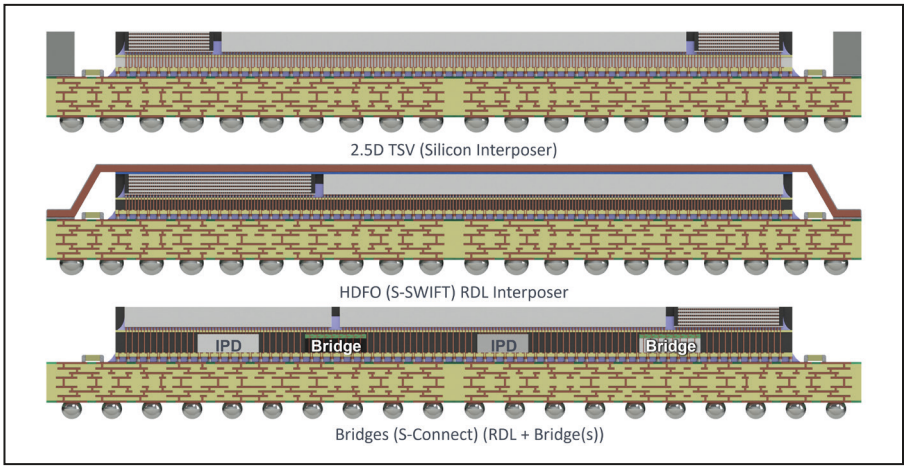


**Figure 1:** High-density module-based products.

## HDFO

Modules based on HDFO interposers have been internally qualified and several of our customers' products are in qualification. Our internal terminology for HDFO is S-SWIFT (Substrate Silicon Wafer Integrated Fan-out Technology). HDFO technology is being applied to many markets and use applications, ranging from high-performance compute and AI, to automotive applications and beyond. Chiplet architectures are leading to a push for advanced packaging design rules that are enabled by HDFO and other module-based solutions. Our fabrication of this HDFO interposer is supported in both a chip-first and a chip-last construction. Each fabrication method has advantages and disadvantages, and in many cases the end customer may have a specific requirement for a given flow or construction.

Chip first, as the words imply, involves the placement of the active silicon chips at the beginning of the module fabrication. Chips are attached face up on a wafer carrier and the multi-layer RDL process is completed with direct metal connections to the active silicon. Chip last involves the fabrication of the RDL first followed by a traditional chip-on-wafer assembly process using solder joints and underfill. Once the modules are completed, they are assembled to a package substrate in a manner similar to non-module-based products. **Figure 2** shows a high-level comparison of these two approaches.

When considering a product intercept into HDFO, we encourage the use of a test vehicle (TV) that matches the design complexity of the final product. This TV phase can make use of the hierarchy of design rules within the design to test boundaries of HVM design rules and overall process capability. This process provides validation for the first product intercept and gives a first check on next-generation requirements. These TV designs utilize a series of daisy chains that can test historical areas of high stress, including die corners, die gaps, module corners, stacked vias and others. Having a well-defined daisy chain can give electrical data that can bolster the mechanical modeling work that is equally critical to the TV phase of development. Predictive modeling can provide key insights to the design and material choices at the start of a program, and it can be valuable at identifying challenges and solutions during development. This TV strategy for development has been used over many successful programs and is highly recommended.

Our current SWIFT technology can support module designs down to 1.5-micron line and 1.5-micron space and with layer counts between 2 and 6 layers. Module sizes can be supported from smaller modules, to modules that are larger than reticle size using reticle stitching. **Figure 3** shows a typical 6-layer RDL module with the top die solder joint fabricated in a chip-last approach. **Figure 4** shows the subsequent module to substrate solder joint.

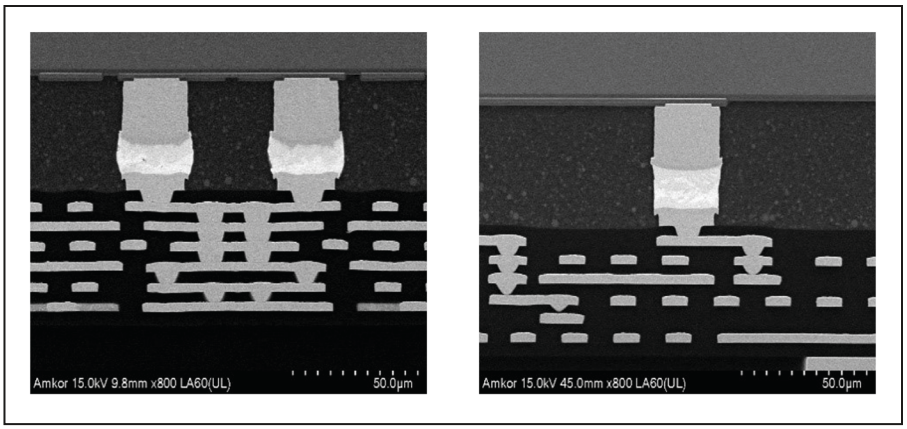


**Figure 3:** Test vehicle die connected to HDFO.

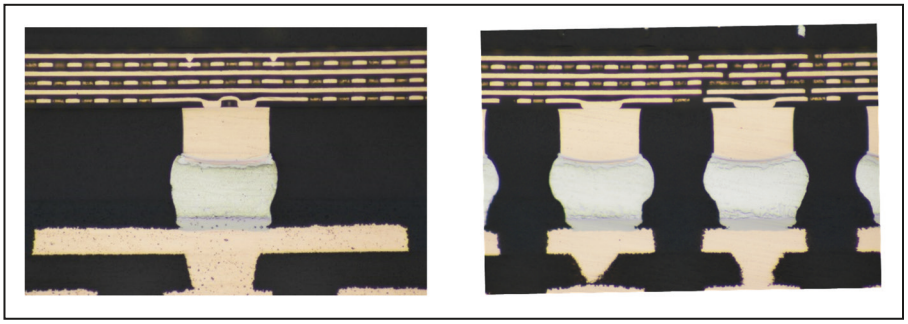

**Figure 4:** Test vehicle HDFO module connected to package substrate.

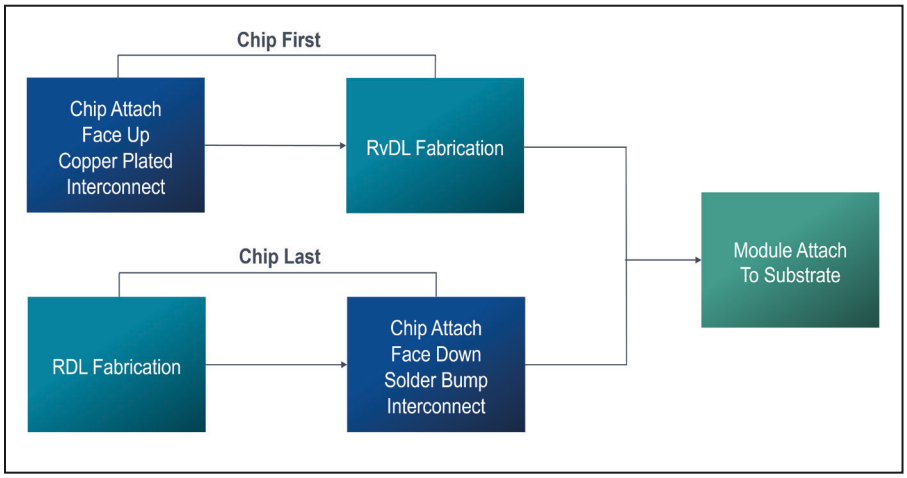


**Figure 2:** General chip-first vs. chip-last flow.

## Bridges

The next iteration of HDFO enables a 3D capability using bridge silicon and other embedded components under the active silicon. The fundamental building blocks developed in HDFO interposer fabrication are extended with the inclusion of embedded bridging components or other devices. These embedded components can have a basic ultra-high density routing function, such as between two chiplets, or they can be active or non-active components, such as an integrated passive device (IPD). The embedded silicon components may or may not contain TSVs allowing vertical connections through the embedded components.

To facilitate this new structure, several key process capabilities are necessary including accurate component placement, tall copper pillar plating, and warpage control. By using this approach, it is possible to utilize the high-density routing capability from the wafer fab to interconnect between chiplets, allowing a reduction in the RDL layer count in the HDFO interposer. The ability to add discrete component functionality is an added benefit for many customers. There exist three primary drivers for S-Connect in the market. First, silicon can offer sub-micron routing capability, which allows denser routing for system design. Second, the use of bridge die for the chip-to-chip connections can reduce the layer count requirement on the HDFO routing for the interposer and increase overall yields. Lastly, the process allows the placement of performance-enhancing non-bridge components such as silicon IPDs, providing closer proximity to key areas of the active silicon.

When engaging with our customers, we consider the tradeoff analysis between HDFO and S-Connect. Sourcing of the silicon bridge and potential IPDs is a key element of this assessment. A supply of these components is as critical to the decision as the active silicon. Process maturity is a key element because the industry has been in production with 2.5D TSV modules for many years. HDFO is, likewise, more mature than the S-Connect technology. These maturity levels can often influence the decision making of our customers.

Our version (S-Connect) of the embedded bridge HDFO module on substrate is shown in **Figure 5**. We have completed internal qualification of a chip-last non-TSV bridge TV, and we are working with several customers on plans to utilize these advanced capabilities.

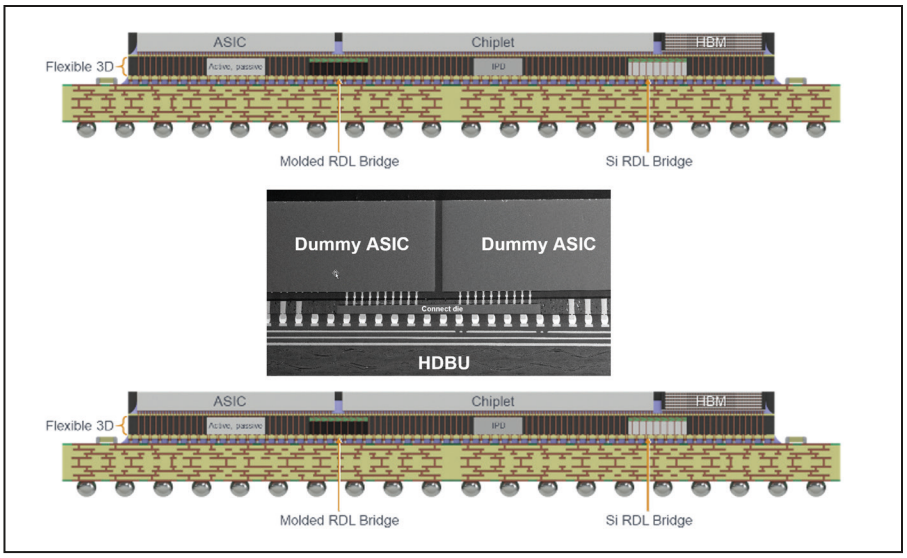


**Figure 5:** Amkor's S-Connect Technology.

## Design support

Our SmartPackage Package Assembly Design Kits (PADK) (**Figure 6**) are ideal for preparing the design layout for a successful supply chain experience. The ability to build the various high-volume or advanced manufacturing and assembly design rule requirements into the design layout early in the design flow process can significantly facilitate a smooth supply chain support path. Notably, this solution is compatible with multiple electronic design automation (EDA) design tools, further securing the ability to align with many independent design workflows.

Two prevalent design workflows in contemporary practices are the Full-OSAT flow and the OEM/Fabless-focused project-based design processes. In the Full-OSAT design workflow, we have comprehensive design services and verification sign-off in accordance with the customer's instructions. In the OEM/Fabless design workflow, we collaborate with users who opt to design their package layout and necessitate the capability to finalize their verification signoffs before providing production data to us for manufacturing and assembly processes.

This ability for accurate implementation of design rules, manufacturing and assembly constraints into the EDA and computer-aided manufacturing (CAM) design tools, with the SmartPackage

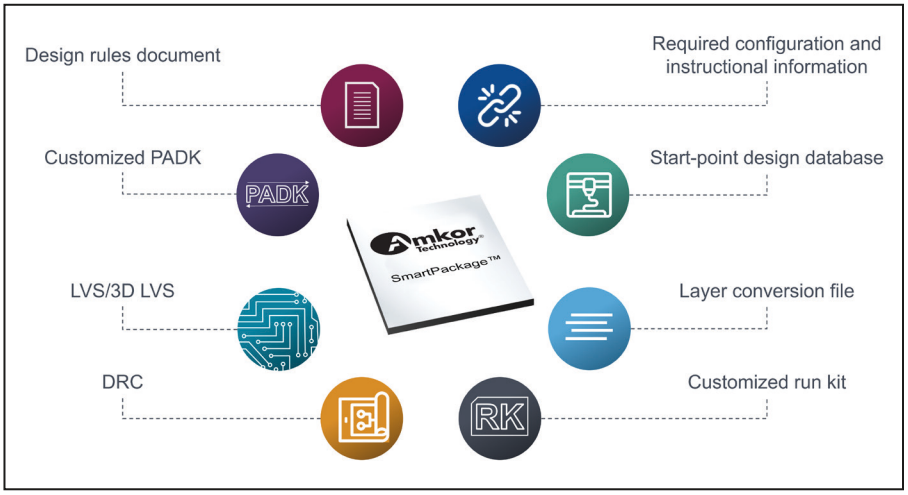


**Figure 6:** Amkor's SmartPackage PADK fine-tuned customized design rule requirements.

PADK enables users to quickly highlight design restrictions early in the design process limiting the number of product design cycles. To experience these benefits, some investment in software and hardware infrastructure may be necessary. Depending on the current design environment, a high-powered Linux server will need to be employed. This system will be tasked with running the extensive manufacturing and assembly design rule constraints on the manufacturing data that is destined for fabrication.

We pioneered the development of PADKs in 2016. Users receive support for PADKs to integrate them as a robust component of their device development approach. The OSAT can provide guidance for package design layout direction, provide specific application training, and provide ongoing design review support, using the latest software to incorporate their packaging knowledge and experience into SmartPackage PADK elements.

Which elements of a package assembly design kit exert the most significant influence on design readiness? The emphasis typically revolves around three key areas. The first is the EDA start-point database, the second is design rules constraint (DRC) sign-off verification, and the third is the ability to validate the production data with the connections list requirements.

A feature of SmartPackage PADK is the capability to fine-tune the specific customized design-rule requirements necessary for the device or design layout needs. The benefit of device-specific design rule decks versus a fixed-node rule deck system is that there is no need to provide careful and extensive waivers to receive a passing verification report.

## Test

We have been providing test services for heterogeneously-integrated products since the inception of the 2.5D TSV development cycle. The systemic approach of designing and evaluating the test vehicles allows test engineers to develop tests for critical aspects of the design before the live product. There are a handful of test challenges that are common to all heterogeneous chiplet packages. Chiplet interconnect integrity is an important one.

Signal and power delivery to every chiplet within the package requires careful layout, design and test during the manufacturing process (**Figure 7**). Package material types used, and the package constructs described earlier in this article, impact the interconnect performance between the chiplets and the pins exposed at the package level. This

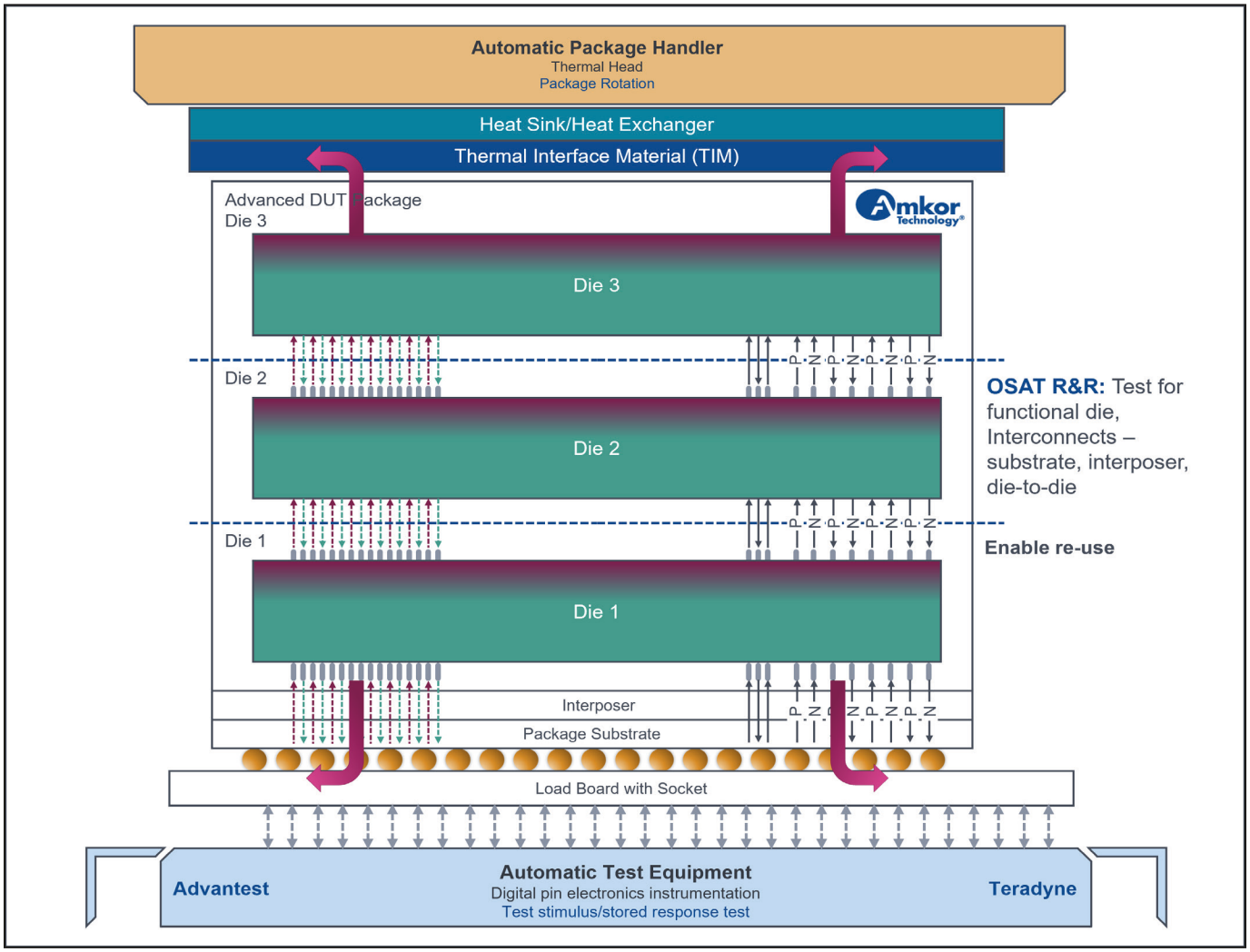


**Figure 7:** Production test for power, data I/O, bias and clocks in multi-die packages.

includes both static connection quality with continuity, leakage and transient ac timing, impedance matching and signal crosstalk. Thermal performance of each of the chiplets also impacts production testing. Thermal gradients due to non-uniform chiplet temperatures are unavoidable. In a carefully designed overall product architecture, design for test (DFT) has access to all functional aspects of the product, which is an important consideration.

IEEE1838 [1] is one such standard that helps during the architecture phase of the product. Test access to each chiplet and all the functional blocks within is a "must have," to allow full production testing.

IEEE-1687 [2] describes the test methodology for accessing instrumentation embedded within a semiconductor device. Electronic data automation (EDA) vendors have defined intellectual property (IP) blocks to monitor environmental attributes including process, voltage and temperature (PVT) on-die. They have a similar concept of adding sensors within the logic design and have documented numerous benefits to the overall manufacturing workflow. PVT sensor placement in the vicinity of the thermal congestion is vital to analyze the severity and sensitivity of thermal densities within the package architecture and design implementation. It is simpler and more cost effective to sprinkle these sensors within the die rather than separately including them on-package. The telemetry stream under various corner cases is read back and analyzed to allow verification against the simulations. **Figure 8** shows a block representation of the Package Environmental Control for monitoring.

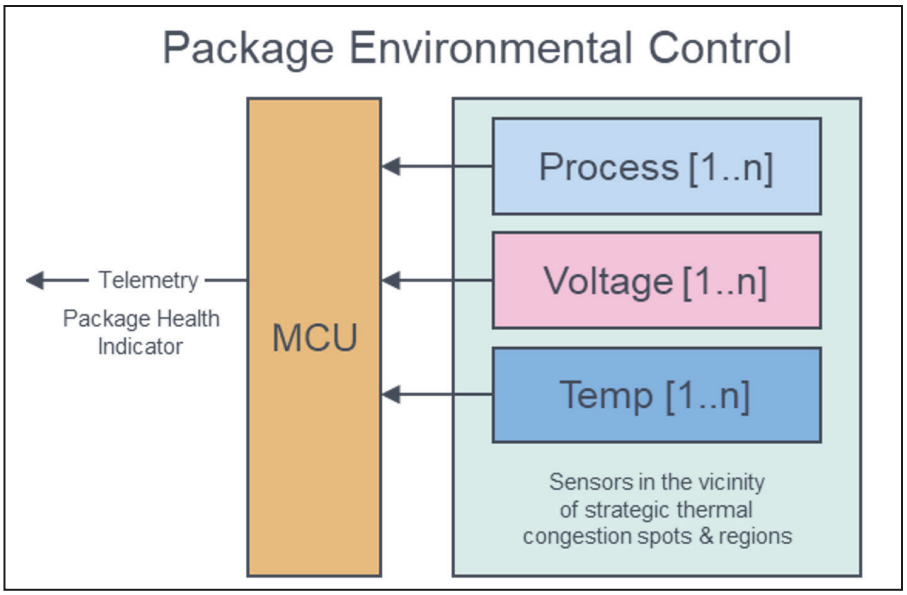


**Figure 8:** Block representation of Package Environmental Control with a variety of sensors that allow a telemetry stream to monitor package health during active operation, including the production test process.

As an OSAT, production test workflow simplification is vital to our company. Industrywide test methodology standardization efforts are helping. For instance, the Universal Chiplet Interconnect Express (UCIe) standard includes constraining the shoreline on chiplets to be fixed. This allows for place and route simplification and interoperability.

The UCIe standard further includes design guidelines for redundancy repair and on-chiplet mission mode eye characterization and margining (**Figure 9**). Redundancy repair allows for yield recovery of packages that would have been a reject without this capability. Eye margining capabilities in production testing, allows the product architects and designers to monitor process variations and make systemic improvements, generation over generation.

A controlled, managed and repeatable production test environment ensures accurate feedback for future product design iterations and consistent yield. The test, package handling and optical inspection supply chain is continuing to refine the metrology to account for all the identified failure pinch points.

## Thermal considerations

Power density continues to increase, and putting more functional silicon into a smaller volume requires close attention to the power dissipation path. We are developing optimized package-level solutions to assist in this effort. Polymer-based thermal interface materials (TIMs) continue to be a mainstay, but for the higher end power levels, metallurgical TIMs may be required, including for 2.5D TSV, HDFO and bridge modules. This is an active area of development.

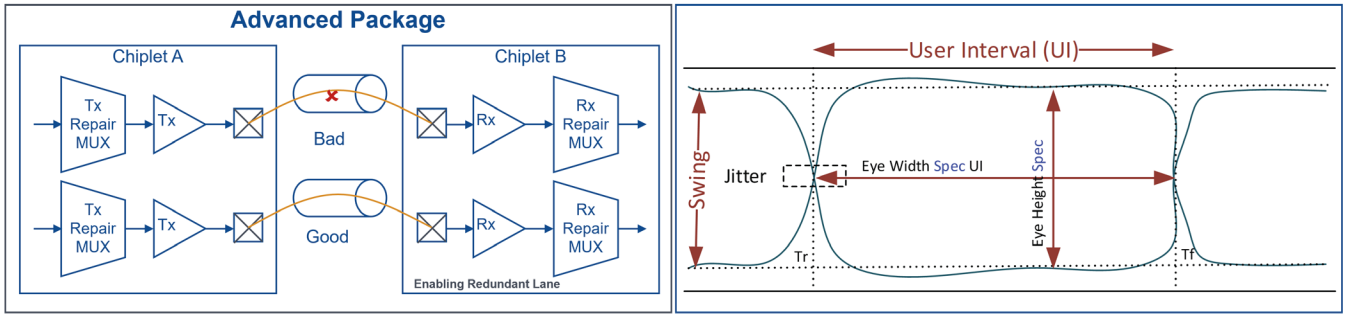


**Figure 9:** Standards are driving provisions for redundant lanes and on-chiplet mission mode eye characterization and margining.

## Summary

The transition to heterogeneous chiplet-based integrations is well underway. The value proposition for the chiplet approach is strong, as evidenced by the recent successful market entries in the compute and AI market spaces. Heterogeneous and chiplet-based IC packaging plays a key role in this evolution, with 2.5D TSV, HDFO and bridge approaches providing a cost-effective path for these integrations.

## Acknowledgments

SWIFT is a registered trademark of Amkor Technology, Inc. S-SWIFT and SmartPackage are trademarks of Amkor Technology, Inc. UCIe is a trademark Universal Chiplet Interconnect Express.

## References

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## Biographies

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