Meeting cost and technology requirements using MLF/QFN

By Marc Mangrum [Amkor Technology, Inc.]

*Micro*LeadFrame (MLF)/quad flat no-lead (QFN) packaging technology is the fastest growing IC packaging solution today. From a market segment perspective, MLF packaging solutions represent more than a 111B-unit market for 2022 across five markets: automotive, consumer, industrial, networking, and communications (Figure 1). The package solution requirements across these markets vary but, the fundamental values the MLF packaging brings to each one is consistently the same: 1) a flexible form factor, 2) adaptable interconnect technology, 3) electrical and thermal performance, and 4) a cost-effective solution.

Flexible form factor

The flexible form factor of MLF packaging enables the technology to service all markets, meeting unique dimensional, environmental and application requirements. In these markets, the MLF packaging solution is being utilized to solve space and functionality challenges. As an example, the capability to form cavities has resulted in the MLF becoming a widely used and versatile solution in the microelectromechanical systems (MEMS) and sensor markets. The automotive industry continues to rely on this technology for solutions in all areas of the automotive electronics deployment. Applications range from infotainment systems to magnetic sensors for steering controls, to even complex moisture sensing systems for automatic windshield wiper systems and battery control management systems. Body sizes ranging from <1.0mm x 1.0mm to >12mm x 12mm are available (Figure 2).

The broad range of JEDEC package thicknesses enables the MLF packaging technology to meet the demanding size requirements of the portable hand-held, Internet of Things (IoT), gaming networking/computer, industrial and the broader consumer markets. Typical body thickness ranges from 2mm to 0.30mm. Ultra-thin capability is also possible down to less than 200µm using both wire-bond and flip-chip interconnect solutions. The thinnest IC packaging solution is the die itself followed by wafer-level chip-scale packaging (WLCSP) and then the MLF over molded packaging technology. As shown in Figure 3, MLF represents the thinnest over molded leadframe technology.

MLF package applications are in almost every electronic system utilized in the world today: radio-frequency ID (RFID), smart home devices, light-emitting diode (LED) bulbs, security tags, electric tools, heating/ventilation/air-conditioning (HVAC) systems, medical devices, satellite systems, audio/visual home electronics, and home and commercial appliances. In any identified electronic product, there is a 99.9% chance a device utilizing QFN packaging technology is in it. The wide use of this packaging technology is not just about body thickness either. Body size, lead

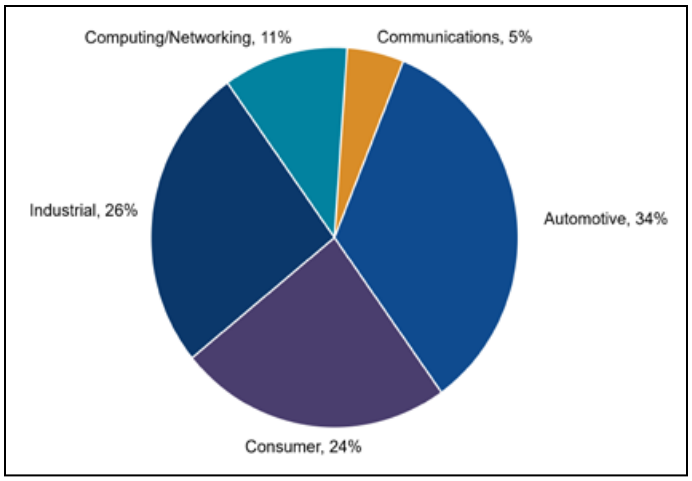

Figure 1: MLF volumes extend across five key market segments.

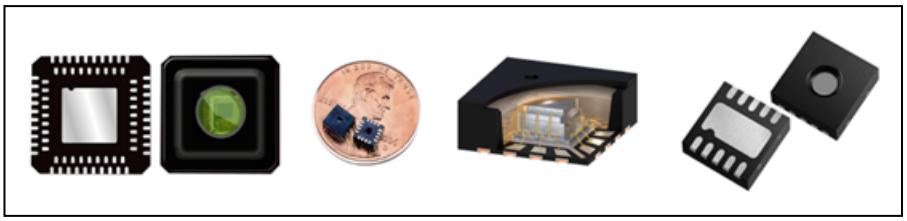

Figure 2: Illustration of the range of body sizes available in MLF packaging.

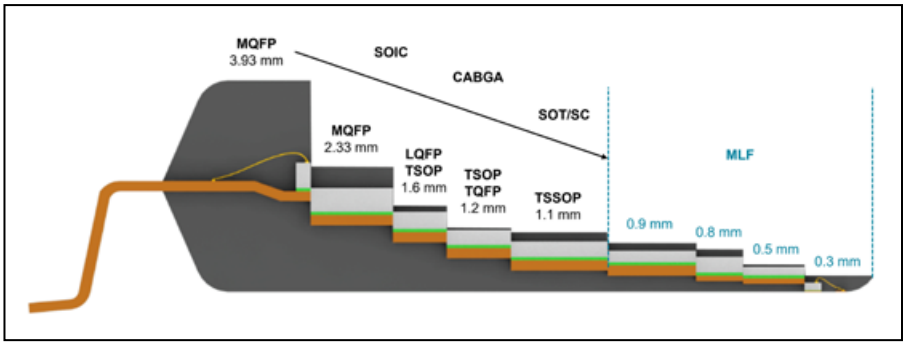

Figure 3: MLF represents the thinnest over molded leadframe technology in the industry.

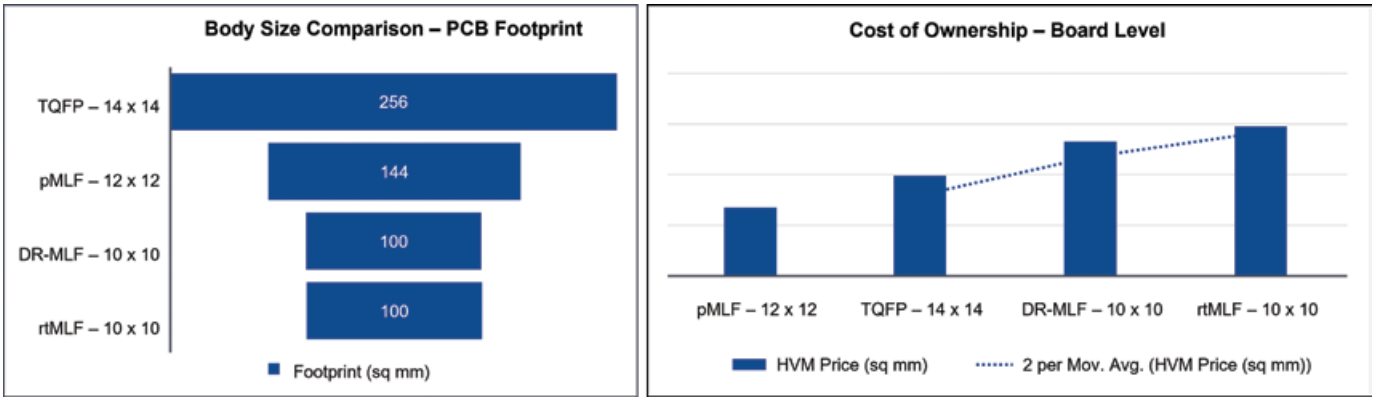

Figure 4: Body size and footprint are critical to application cost.

count, and flexible lead designs are also key attributes that have led to the use of this IC packaging solution in a variety of semiconductor applications.

Cost-effective solutions

Body size or footprint are of equal importance to all applications (Figure 4). Known as the cost of ownership (COO), the amount of area on the printed circuit board (PCB) of a given application is critical to the cost of the application solution. So, it is not only how thick the package is today, but how large it is that can become more of a priority consideration. Migration paths from laminate carrier array ball grid array (CABGA) and quad flat pack (QFP) packages are often driven by these two advantages of the MLF technology. Other COO considerations seen with MLF packaging are the stencil costs, the solder usage, solder joint reliability, and the ability to inspect the solder reflow process by monitoring the lead fillet formation.

Higher pin count requirements are possible for MLF packaging technology by the use of multi-row, interstitial lead designs. Known as the Dual Row MLF (DR-MLF) package, this format can increase the I/O count of a given body size by as much as, or more than, 50%. This enables MLF technology to add functionality within an application while maintaining a small PCB footprint. The DR-MLF is available in both saw and punch formats, with the punch format utilized extensively for body sizes of 8mm x 8mm and greater. Along with the higher I/O density, the DR-MLF also has the advantage of better thermal performance than other equivalent lead solutions such as a laminate CABGA and has demonstrated excellent board-level reliability (BLR) performance. Long a concern with the interior row of leads, data taken to determine solder joint reliability shows that DR-MLF packaging is capable of the same BLR performance as the single-row versions. This has led to the recent adaptation of the DR-MLF technology into automotive applications.

Another way to increase the I/O count of the MLF package is by reducing the lead pitch. Today, the fine-pitch version of the MLF design is available from 0.5mm pitch down to 0.30mm pitch. This enables the package to retain a single-row configuration while increasing the I/O count by more than 30%. Seen as an advantage in computing and consumer electronics applications, the ultra-fine pitch designs at 0.35mm and 0.30mm can be a challenge for electrical test, as well as for the PCB layout and the surface mount technology (SMT) process. Fine-pitch contactor solutions for these pitches are a challenge as is the electrical performance boards required to interface with the automatic test equipment (ATE) tester. High-quality solder stencils and high accuracy of device placement are needed to minimize the incidence of solder shorting during reflow (Figure 5). However, the advantages of these very fine-pitch solutions are seen where size, thermal performance and I/O level are justified by the critical and necessary requirements of the actual application use cases. The use cases in the networking and computer markets are the primary drivers for these fine-pitch solutions. Hard disk drive and solid-state drive (SSD) controllers are primary use cases benefiting from this ultra-fine-pitch version of MLF technology.

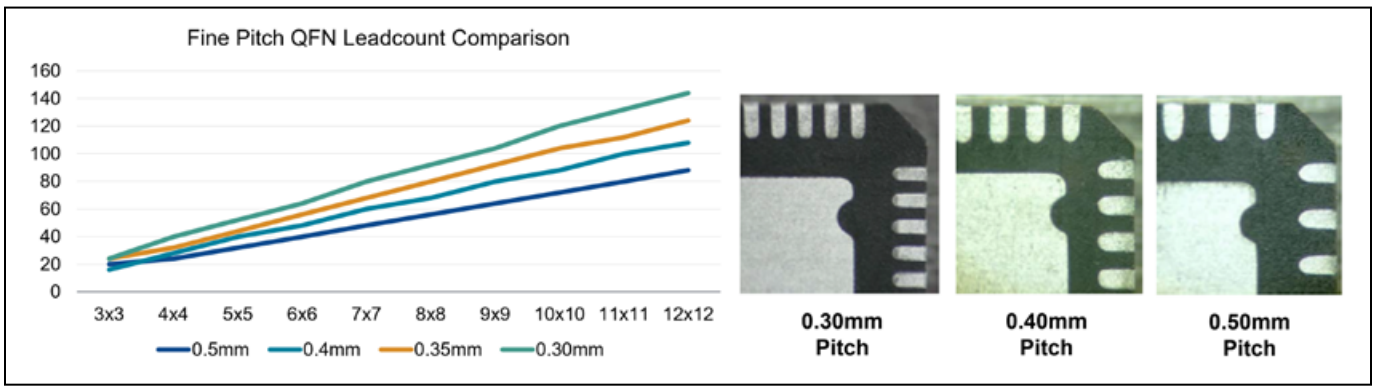

Figure 5: Illustration demonstrating fine-pitch progressions.

Extended electrical and thermal performance

The flexible lead configuration has enabled the MLF packaging technology to extend its capabilities for providing solutions in the power market. The Power QFN (PQFN) is a variant of the saw MLF technology that enables multiple customer exposed pads with multiple fused leads. Combined with the integration capabilities of copper (Cu) clips and heat slugs, the PQFN packaging solution has the thermal capability needed for power metal-oxide semiconductor field-effect transistor (MOSFET) designs while retaining the advantages of size (body thickness and body size). The split exposed pad capability is also a primary reason the MLF is finding success in the GaN market, especially for multi-die solutions where the gallium nitride (GaN) die and an application-specific integrated circuit (ASIC) are integrated into a common package (Figure 6). These solutions are rapidly finding their way into portable, handheld devices and electronic charging devices of all kinds.

Solder die attach, as well as sintering paste, have further extended the thermal performance of PQFN solutions. Even mixed materials such as epoxy die attach for the ASIC controller die and solder paste for the MOSFET attach are common. Isolation of the gates in MOSFETs is also a possibility and an advantage of the split-pad design capability of this packaging technology. Thermal dissipation for properly configured PQFN devices is noted to be extremely robust. With the embedded heat slug and external heat sink, devices capable of a continuous drain current of 15 amps and drain to source voltages of 150 volts can be sustained. The use of Cu leadframes, and lead-free solders are key components of this packaging solution that enable the on-resistance (Rds(ON)) performance required for devices with demanding high-power requirements.

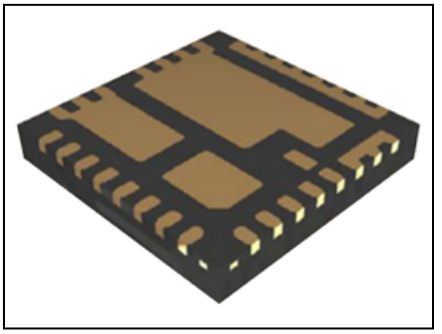

Figure 6: Split die attach pad showing isolation of the ASIC from the GaN.

Adaptable interconnect technology

Further versatility of the MLF technology is demonstrated by the multiple interconnect solutions that have been proven and are available in the market today. These range from traditional wire bond designs to high bump count Cu pillar flip-chip designs. The use of gold (Au), Cu and silver (Ag) wires of various diameters addresses the requirements for performance and cost, while enabling the broad interconnect solutions for a variety of wafer technologies such as silicon, GaN, and silicon on sapphire (SOS), with technology nodes ranging from 120nm to 7nm. Wire diameters range from 0.6mil to 2.0mil. This wide range of wire diameters supports device-level functional performance needs while enabling the right cost point for the solution for the die technology node.

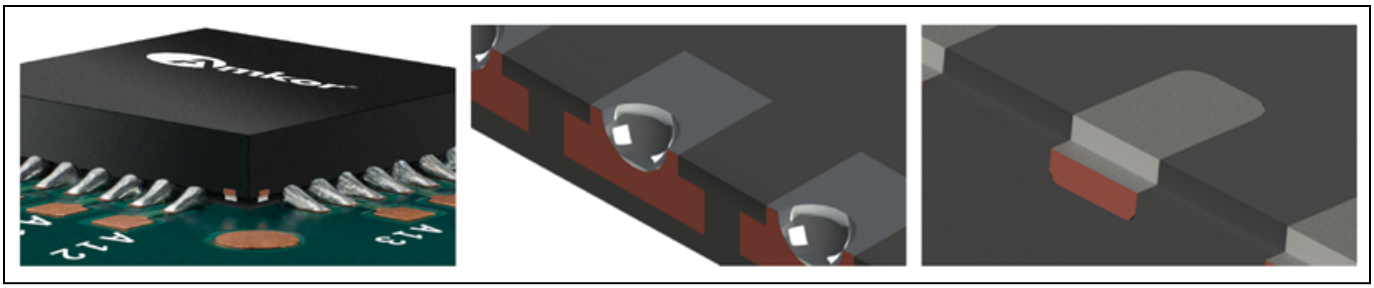

Figure 7: Wettable flank addresses critical needs of the automotive original equipment manufacturers's (OEM's) manufacturing process.

The flip-chip capability of the MLF technology enables size reduction while improving electrical signal integrity and thermal performance. Applications such as power management integrated circuits (PMICs) and radio frequency (RF) are early adopters of the leadframe flip-chip solution. Typical flip-chip MLF technology designs today that utilize Cu pillar bumping can have 160µm bump arrays. RF devices rated up to 40GHz utilize this type of packaging solution in applications ranging from smartphones to high-speed servers. The use of a Cu leadframe enables thermal performance in excess of 4 watts, making this technology ideal for the battery management systems in wireless/handheld applications. Adaptation of the flip-chip MLF is occurring in automotive applications as well. As the battery electric vehicle (BEV) market grows, more focus is being placed on size and weight of the electronics in the vehicles. Battery management controllers today are predominately hard wired into the battery cell. The transition to wireless control solutions will require more devices, so, having small, low weight packaging solutions is of paramount interest.

The exposed die attach pad (either top or bottom, or both) feature enables this packaging technology to meet the thermal needs of high-performance networking devices as well as power devices. The ability to integrate large-diameter bond wires and Cu clips for power field-effect transistors (FETs) has enabled MLF packaging solutions to extend into high-power applications and meet the very demanding market requirements ranging from automotive to consumer gaming products.

New material sets specifically target zero delamination and the demanding automotive reliability requirements of the Automotive Electronics Council's AEC-Q100 and AEC-Q006 standards. These material sets have also extended the use case of this technology to applications previously dominated by leaded-package solutions such as QFPs and small outline integrated circuit (SOIC) designs. Roughened leadframe finishes, improved epoxy die attach materials, film die attach for automotive applications and improved molding compounds to enhance Cu wire performance are only a few of the enhancements that are being applied to extend the value of the MLF packaging technology. Considering the ever-rising increase in the price of Au, more than ever IC packaging solutions need alternatives for interconnects. The automotive industry has been reluctant to adopt Cu wire too quickly primarily due to issues seen regarding long-term latent failures of the wire bonds attributed to interactions of the mold compound and the Cu wire. Innovations in both the wire and mold compounds have resulted in the much-improved performance seen with respect to the reliability requirements and have led to a broader adaptation of Cu wire for automotive ICs.

One of the key recent innovations with respect to MLF technology is the wettable flank (**Figure 7**). Because the MLF is a leadless package and the automotive industry requires a visible indicator of a reliable solder joint post reflow, the need for an inspectable solder fillet on each lead is mandatory. This is especially important in automotive applications where each PCB is inspected using automated optical inspection (AOI) equipment. The formation of a solder fillet on each lead that can be detected by the AOI equipment is critical to the automotive OEM's manufacturing process. MLF packaging solutions form the fillet using a process known as step cut in the saw singulation process, or the dimple when punch singulation is applied. Both processes enable the formation of a fillet necessary for indicating proper wetting of the leads and both processes are widely utilized in the automotive industry today.

Summary

The MLF/QFN technology is a market adaptable and cost-sensitive technology. Utilizing the flexible form factor and adaptable interconnect capabilities in combination positions this packaging technology to meet a multitude of market needs and application requirements.

Acknowledgments

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Biography

Marc Mangrum is Sr. Director for MLF® Products at Amkor Technology, Inc. Tempe, AZ. Prior experience includes more than 30 years at Motorola and Freescale. His capabilities include the development of advanced ATE for digital/analog ICs, and cost-reducing IC package design and assembly processes. He has published over 30 papers and has 33 patents issued, and is a graduate of the U. of Texas at Austin with core competencies in mathematics, electrical engineering, and business administration. Email Marc.Mangrum@Amkor.com

Enabling **performance.**

*Micro*LeadFrame® (MLF®/QFN) provides the right size, weight and performance for automotive, consumer, industrial, networking and communications application requirements. Our innovative leadframe packaging technology offers a cost effective solution when flexible form factor, adaptable interconnect technology, electrical and thermal performance are required.

Amkor – your source for leadframe packages.

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