Wafer Level Void-Free Molded Underfill for High-Density Fan-out Packages

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Abstract

In this study, experiments and mold flow simulation results are presented for a void-free wafer level molded underfill (WLMUF) process with High-Density Fan-Out (HDFO) test vehicles using a wafer-level compression molding process. The redistribution layer (RDL)-first technology was applied with 3 layers of a fine-pitch RDL structure. The test samples comprised 11.5 x 12.5-mm^2 die with tall copper (Cu) pillars around the die. Destructive analysis was used to clearly inspect MUF voids on the whole wafer area. The molded wafer was ground to the bump area where the MUF voids exist using a mold grinding machine and MUF voids were inspected through a high-resolution scope.

The WLMUF characteristics of the conventional compression molding process with various epoxy molding compound (EMC) types have been investigated. A void-free WLMUF process was achieved by applying an optimized EMC dispensing method and parameters. These results are verified through the mold flow simulation, which correlated to the experimental results. Finally, the void-free WLMUF HDFO samples passed reliability tests of temperature cycling (TC), high temperature storage (HTS) and Unbiased Highly Accelerated Stress Test (UHAST) after moisture resistance test (MRT) Level 3.

Keywords: High-Density Fan-Out, Wafer Level Packaging, wafer-level MUF, compression mold, mold flow simulation

Introduction

Wafer level High-Density Fan-Out (HDFO) packaging is attracting a lot of attention in mobile, artificial intelligence (AI) and big data applications due to its ability to support high input/output (I/O) count and high performance. Such devices can be made using two method called Chip-first or redistribution layer (RDL)-last and Chip-last or RDL-first technology. Due to the production yield, the Chip-last or RDL-first technology is being introduced to the industry [1]. This technology uses the capillary underfill (CUF) and overmold process. However, the CUF process is one of the slowest processes in Wafer Level Packaging (WLP) due to the unit-by-unit manner and inherent capillary flow characteristic of the CUF process [2] resulting in low throughput and higher assembly cost. To overcome this challenge, the WLMUF process is proposed by replacing CUF and overmold process to one-step process. The main benefit of the wafer level molded underfill (WLMUF) process is faster throughput. As the die per wafer (DPW) increases, this benefit will be larger. A further advantage is the smaller form factor compared to the CUF application. Due to underfill fillet length consideration in package design, there should be minimum clearances between die edge to package edge, die to die for multi-die and adjacent passive components in a System-in-Package (SiP) [3]. In wafer format, higher throughput and lower assembly cost can be achievable by introducing a WLMUF process.

There are several studies about WLMUF processes that achieved void free results with mold parameter optimization such as compression pressure, stage transfer speed and vacuum pressure, etc. [4]. However, WLMUF characteristic and quantitative analysis of WLMUF voids on experimental results have not been clearly introduced.

This paper presents the physical WLMUF gap filling characteristics for all units on a whole wafer with the conventional compression molding process. The 11.5 x 12.5-mm^2 test chip was flip bonded for the WLMUF tests. The test chip on the wafer was molded and the wafer was ground for MUF void inspection. The quantitative analysis was conducted to address each void position and its size. Various epoxy molding compound (EMC) types with different viscosity were tested and the results showed the limitation of void-free WLMUF with a conventional compression molding process. To overcome the limitation, a new dispensing pattern with optimized parameters was tested. In addition, a wafer level mold flow simulation was conducted in accordance with experiments results.

Experimental

A. Test vehicle design & unit array

A cross-sectional schematic diagram of the test vehicle is illustrated in Fig. 1 (a). The test vehicle is a flip-bonded HDFO package and consists of 11.5 x 12.5-mm^2 top die (b) on 14.5 x 16.5-mm^2 bottom HDFO RDL section with tall copper (Cu) pillars.

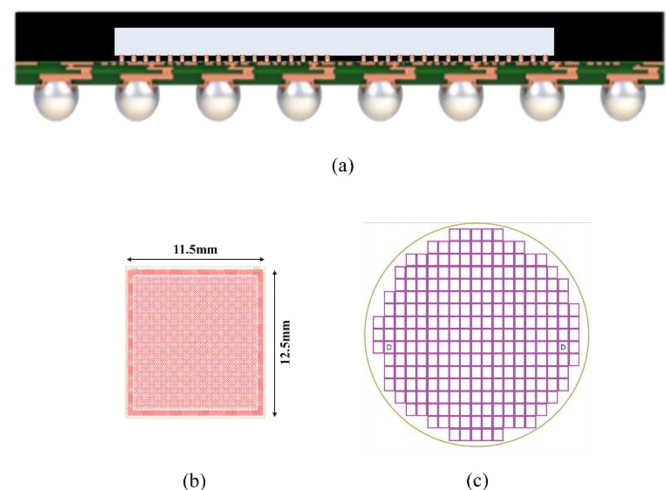

Fig. 1. (a) Package cross-sectional schematic diagram, (b) chip design and (c) unit array in a wafer.

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A 40-µm thickness of the RDL-first technology with 3-layer RDLs and 5 x 8-µm line width/line space is applied. Tall Cu pillars are embedded in a Package-on-Package (PoP) application, where the tall Cu pillars enable vertical interconnections between the RDL and the top package. The tall Cu pillar with 200-µm diameter and 300-µm pitch is placed in 3 rows in the horizontal direction and in 1 column in the vertical direction. The minimum distance from the die edge to the tall Cu pillar is 450 µm. A 100-µm thick top die was applied for the over-mold structure which has a 30-µm bump gap. The bump diameter is 70 µm with a 110-µm minimum bump pitch and a total bump I/O count of 8600. A total of 243 units were in WLMUF test (c) with 17 lows and 18 columns.

B. Test process flow

The process flow of a wafer level MUF is described in Fig. 2, where a chip-attached wafer is prepared for WLMUF tests. The molding process used a wafer level compression molding machine which is commonly used in wafer level package. EMC was dispensed at the wafer center by a target amount.

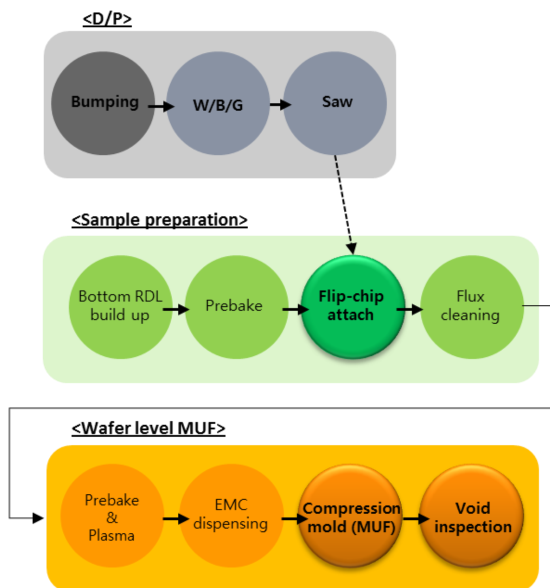

Fig. 2. Wafer level MUF test process flow.

The chip-attached wafer was loaded to the bottom mold chase as shown in Fig. 3 (a). The top and bottom chases are clamped and a low vacuum pressure is presented for void minimization. Then, the bottom mold chase is moved up for EMC spreading (b). Finally, the EMC touches the cavity edge and was compressed and cured (c).

C. Wafer level MUF void inspection

In the development of the void-free WLMUF process, inspection of the entire wafer area is essential. One of the void inspection methods uses scanning acoustic tomography (SAT). SAT can inspect voids without damaging the package. However, it is difficult to detect voids below 100 µm on an over-molded package. Also, it takes considerable time to scan the whole wafer area with SAT. So, generally, the parallel lapping (P-lapping) method has been used to remove the top die and to precisely check for voids on a specific unit after package singulation for comparison with SAT.

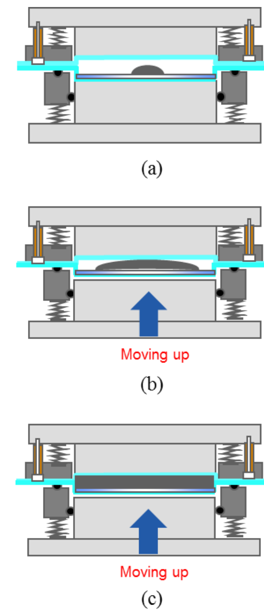

Fig. 3. Wafer level compression molding process: (a) wafer loading, (b) EMC moving and (c) EMC compression and curing.

In this study, a wafer level mold-grinding process is adapted to remove all dies at once without package singulation and to observe WLMUF voids as shown in Fig. 4. After the WLMUF process, (a) the wafer was ground to bump area (b) and all units were revealed. Then, MUF voids were inspected using a high-resolution microscope (c) for all units on the wafer. The void position was characterized on the wafer and its size was analyzed.

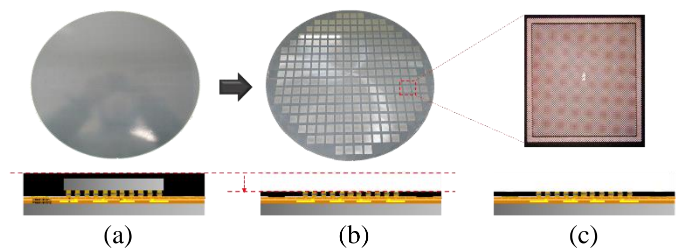

Fig. 4. Void inspection process: (a) molded wafer, (b) mold grinding to bump area (p-lapping) and (c) visual inspection.

Results and discussion

A. Wafer level MUF gap filling characteristic

Wafer level compression mold is a transfer-like mold process because EMC is moving from wafer center to the edge as the bottom chase moves up. So, the wafer level gap filling characteristics can be affected by unit position. Therefore, it is

important to know how to fill the gap under the die with EMC during compression molding process. After revealing the die, mold flow could be predicted through the flow mark of the EMC. The flow mark of the EMC at each position on the wafer is shown in Fig. 5, the center (a), middle (b) and edge (c) of the wafer. From the X shape of the flow mark, it can be assumed that EMC surrounds the die and EMC starts to fill the die from each die edge by the compression force and finally completely fill the gap under the die making the X shape of flow mark. At all unit positions, the same flow mark shape was observed. It is expected that each unit has the same gap-filling characteristic even though EMC is moving from the center to the edge.

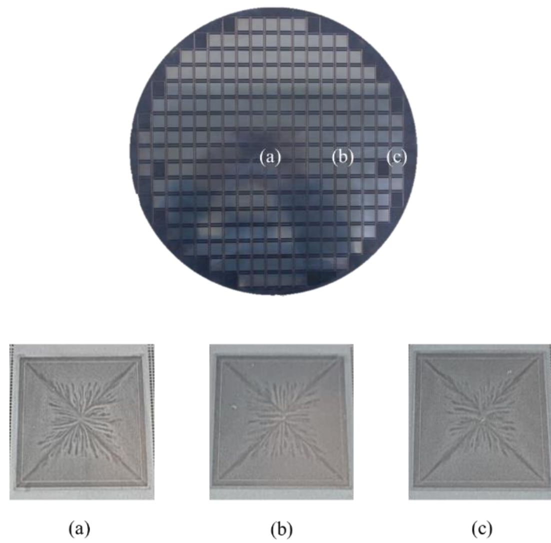

Fig. 5. Flow mark of: (a) wafer center unit, (b) middle unit and (c) edge unit.

B. Wafer level MUF characteristics depend on EMC viscosity

Low viscosity EMC was reported to have a better gap-filling performance [5]. However, quantitative analysis has not been addressed, such as how many voids occur and what void sizes are observed on a whole wafer. Three types of EMC having different viscosities were chosen for the MUF evaluation as listed in Table 1. Viscosity of the 3 EMCs are high, medium and low, respectively, and all EMCs have the same max filler cut size.

Table 1. EMC properties

EMC material	EMC-1	EMC-2	EMC-3
Filler contents (%)	80	80	78
Max filler (um)	5	5	5
Viscosity (Pa·s)	High	Medium	Low
Tg (°C)	160	165	168
CTE1 (ppm)	11	13	11
CTE2 (ppm)	46	48	30
Flexural modulus (Gpa)	16	13	9

The MUF process was conducted using the same mold parameters to understand the viscosity effect on WLMUF performance. After compression molding, the wafer level mold grinding process was performed to reveal all the die on a wafer as shown in Fig. 6.

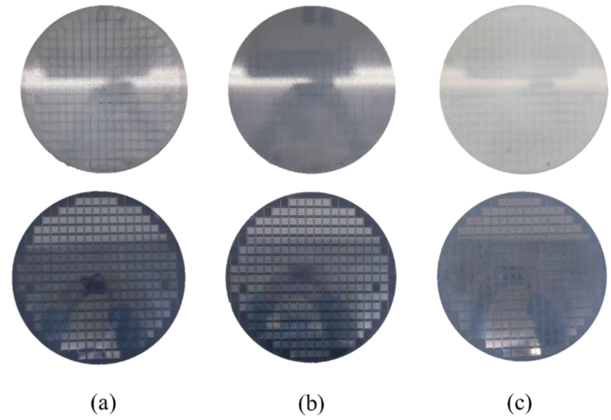

Fig. 6. Molded wafer and ground wafer of: (a) EMC-1, (b) EMC-2 and (c) EMC-3.

The void inspection results depending on the EMC viscosity are shown in Fig. 7. The void location was colored and void size was indicated from green to yellow to red as the void size increased.

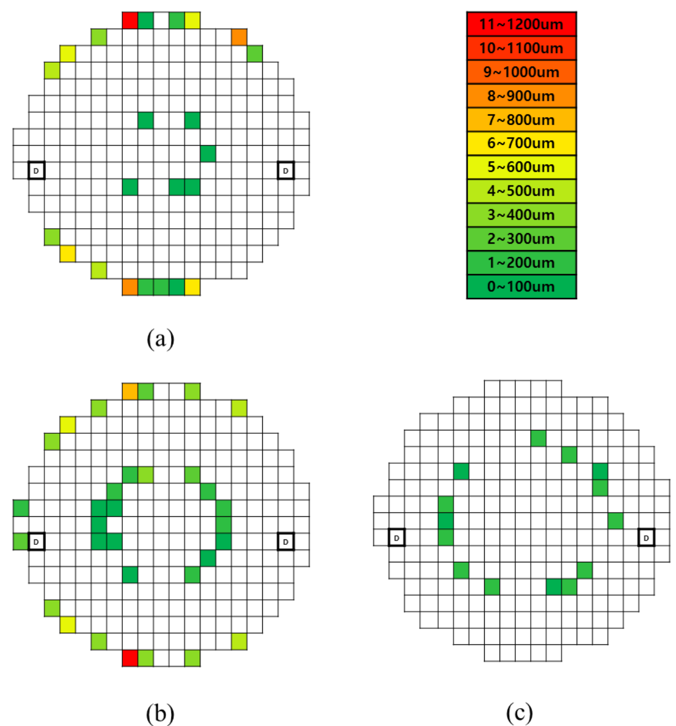

Fig. 7. Void distribution and void size of: (a) EMC-1, (b) EMC-2 and (c) EMC-3

A void size distribution Fig. 8 (a) and average void size (b) was analyzed in terms of EMC viscosity. It was clearly observed that the lower viscosity EMC (EMC-3) has the best MUF performance. Higher viscosity EMC (EMC-1 and EMC-2) had a wider void size distribution from 100 μm to 1200 μm and lower viscosity EMC (EMC-3) had a narrower void size distribution from 100 μm to 200 μm. Also, when the EMC viscosity decreased, the average void size decreased.

The void position can be classified into two types: inner area void and outer area void. The EMC-1 and EMC-2 had both inner and outer area voids and EMC-3 had only inner voids. The void size at the outer area was bigger, while void size at the inner area was smaller. The maximum void size at the outer area was 1200 μm and 300 μm at the inner area, respectively. This result is expected to be related with viscosity transition from low to high viscosity during the EMC flow from the wafer center to the wafer edge. Because the EMC is continuously exposed to the heat from the bottom and top chases, the EMC viscosity can be higher at the outer area resulting in larger voids.

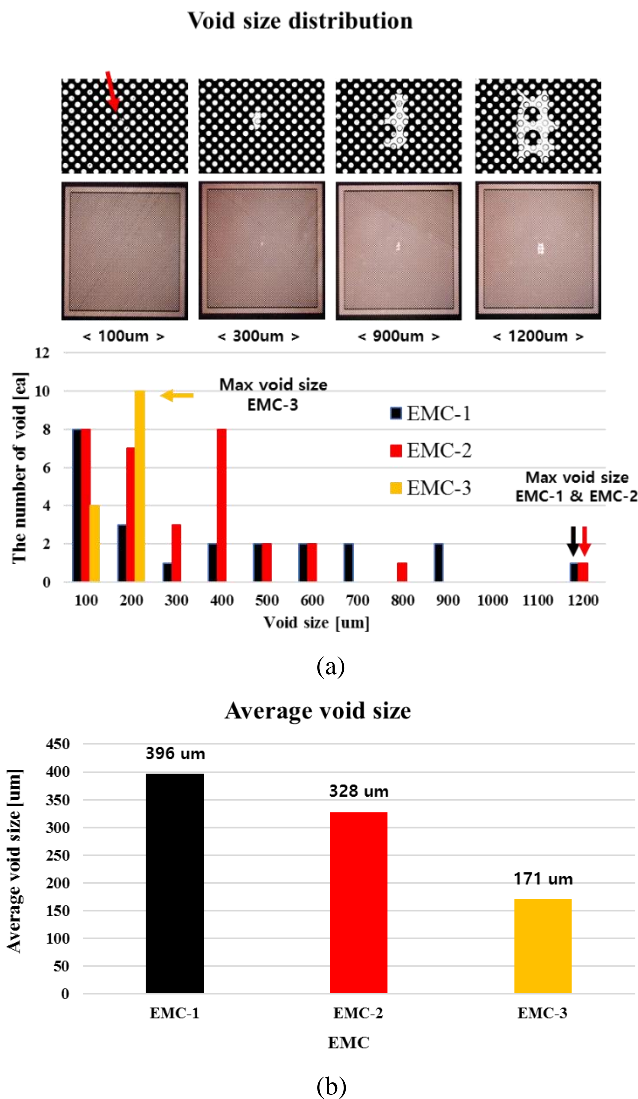

Fig. 8. (a) Void size distribution and (b) average void size.

Although EMC hardening is expected to be a dominant factor for voids, mold flow also can be one of the main factors considering the large void location. Most of the large void locations are positioned at diagonal and vertical directions, colored as yellow to red rather than vertical or horizontal direction. This implies that when EMC flows over the die in a diagonal and vertical direction, there is a greater possibility of void generation.

C. Void-free wafer level MUF solutions

The challenge of the wafer-level MUF with conventional compression molding process was addressed in previous section. With the conventional compression molding process, EMC was dispensed at wafer center area and spread to cavity edge resulting in MUF void. To overcome this challenge, new dispensing patterns and parameters, such as transfer speed and compression force, were tested.

One of the new dispensing patterns with optimized parameters achieved a void-free WLMUF result. The MUF result was inspected after p-lapping using a wafer level mold grinding process. The p-lapping result is shown in Fig. 9. The representative quadrantal wafer image clearly shows the void-free WLMUF results. The unit positions where the largest MUF voids occurred also showed void-free results.

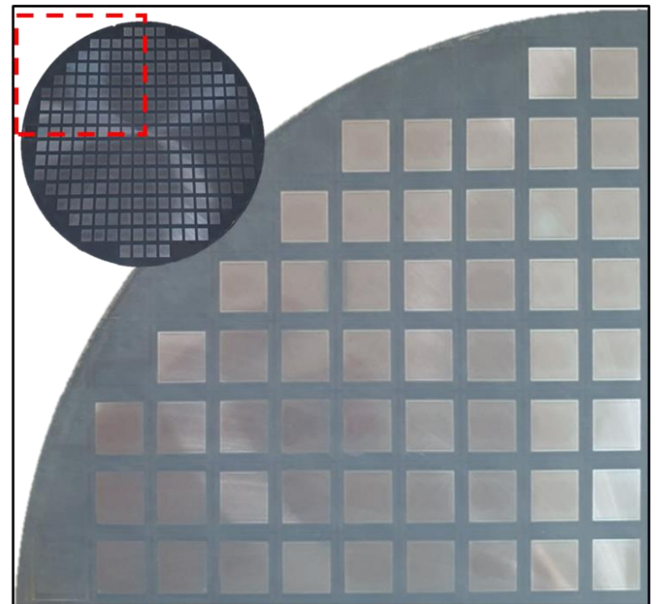

Fig. 9. The representative quadrantal wafer image.

The detail p-lapping results of the unit are shown in Fig. 10 for wafer center, middle and edge. Regardless of the unit's position, p-lapping images show void-free results.

Also, this image shows the void-free results even though it has tall Cu pillar around the die. Basically, the tall Cu placement is based on the CUF process. For the CUF process, under-fill (UF) dispensing area and fillet length consideration are necessary so the UF does not touch the tall Cu area because this can cause UF backflow from the die and result in an unstable UF process. However, in the MUF application, these design considerations are unnecessary. Thus, package design can be reduced by

decreasing the die to tall Cu distance and more DPW are achieved.

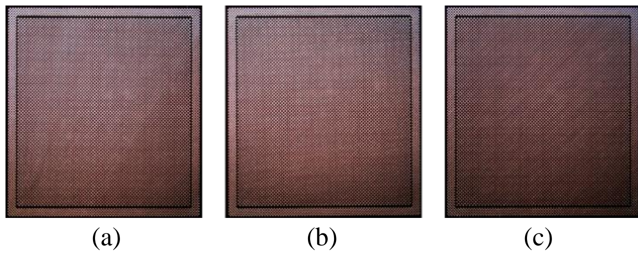

Fig. 10. P-lapping image of (a) wafer center unit (b) middle unit (c) edge unit

Cross sectional analysis was performed to check the filler separation between bump and bump. The die edge and center area were inspected as shown in Fig. 11. The 30-μm gap under the die is filled with EMC and there are no signs of filler separation.

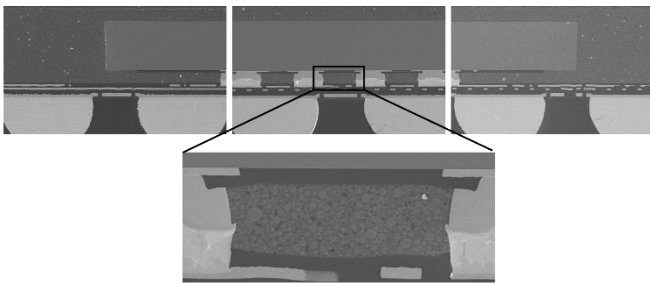

Fig. 11. Cross-section image.

D. Mold flow simulation

The void-free WLMUF was verified through mold flow simulation. The real challenge for simulation is the bump geometry. Thousands of bumps are included in one package due to the high I/O trend. Hence, it is not practical to simulate 12-inch wafer with fully populated packages due to computational resource limit as well as time cost. So, in this mold flow simulation, only a quarter of a wafer was studied as shown in Fig. 12.

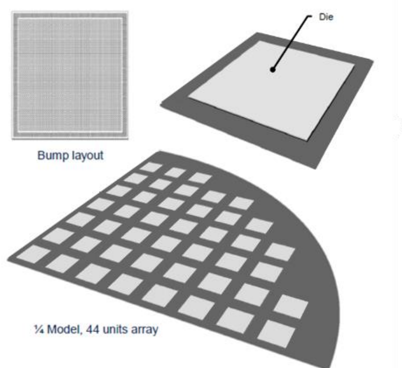

Fig. 12. Mold flow simulation model.

Firstly, the MUF characteristics with compression molding process was observed as shown in Fig. 13. The EMC surrounded the die and EMC started to fill the gap under die from all die edges and completely filled the gap under the die with the compression force. There is void filling time difference depending on unit position due to EMC flow, but the EMC flow is the same at all positions. As expected from the flow mark inspection, the simulation results also showed that EMC covered over the die first and then started to fill the gap under die regardless of the unit's position.

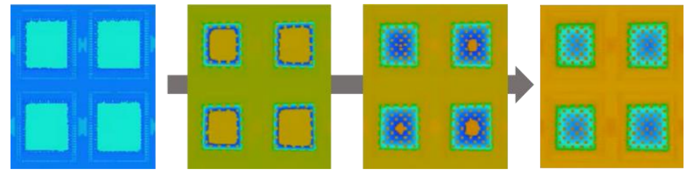

Fig. 13. The MUF characteristic with compression molding process.

WLMUF simulation results are shown in Fig. 14. The results show the difference between (a) conventional dispensing pattern and (b) new pattern with optimized parameters. It is noted that the mold flow simulation results on the new pattern showed the void-free results corresponding to experimental result.

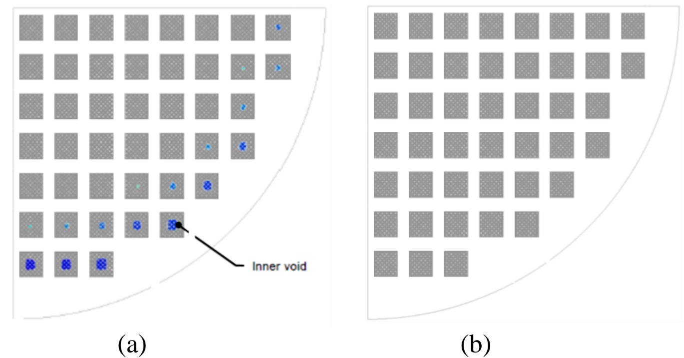

Fig. 14. Mold flow simulation results depending on dispending pattern: (a) conventional and (b) new pattern.

The conventional mold had 0.8% of void volume out of the total EMC volume and new pattern had 0% void volume as shown in Fig. 15. Also, the conventional dispensing pattern had a similar result with experimental results in void position and most of the voids are observed at the wafer edge area. Furthermore, the location where the largest void occurred was in a good agreement with experimental results. The largest void is found at the diagonal and vertical direction compared to horizontal direction at mold flow simulation.

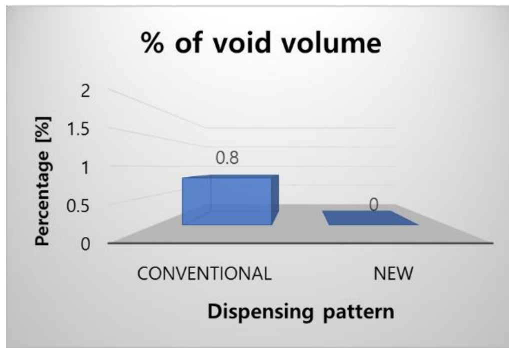

Fig. 15. Void volume comparison depending on EMC dispensing pattern.

E. Reliability result

Component level reliability (CLR) testing was conducted for the WL MUF test vehicle with 3 layers of RDL-first technology. The reliability testing was done in accordance with the JEDEC standard conditions. To verify the reliability of the WLMUF, daisy chain die were subjected to open/short tests. The WLMUF test vehicle passed all tests without any issues. Table 2 shows the reliability test items, conditions, sample size and results.

Table 2. The CLR test conditions and results

No	Reliability test items	Test condition	Readout point	Sample size	Results
1	Precon (L3)	L3/260℃	-	180	Passed
2	uHAST w/ L3	130℃/85RH	192hrs	60	Passed
3	TC 'B' w/ L3	-55℃/125℃	1000 X	60	Passed
4	HTS	125℃	1000 hrs	60	Passed

Conclusion

In this study, void-free WLMUF with a compression molding process has been successfully achieved using an optimized dispensing pattern and parameters. Void inspection on all wafer units after die revealing led to the clear understanding on WLMUF gap filling characteristics and WLMUF performance depending on the EMC viscosity. A low viscosity material had better gap filling performance however, also showed the limitation of WLMUF with conventional compression molding process at the same time.

An optimized dispensing pattern with optimized parameters provided the void-free WLMUF result. All die at different positions had the same MUF performance. The WLMUF with tall Cu around die showed the possibility of the smaller package design with WLMUF leading to higher DPW and lower process cost. The void-free WLMUF result was validated through the mold flow simulation that corresponded to the experimental results.

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