Enabling the 5G RF front-end module evolution with the DSMBGA package

By Curtis Zwenger [Amkor Technology, Inc.]

With the rise of 5G wireless technology, cellular frequency bands have increased considerably, requiring innovative solutions for the packaging of radio frequency (RF) front-end (RFFE) modules for smartphones and other 5G-enabled devices. Our double-sided molded ball grid array (DSMBGA) is an example of such solutions. Double-sided packaging technology has vastly increased the level of integration for RF front-end modules used in smartphones and other mobile devices. Common RF front-end modules consist of a low noise amplifier (LNA), power amplifier (PA), an RF switch, RF filters and duplexers.

Advanced system in package (SiP) design rules and DSMBGA technology enable the integration of additional components – such as antenna tuners and passive components – freeing up premium device motherboard real estate.

5G overview

5G is the fifth-generation technology standard that cellular phone companies began deploying worldwide in 2019. It includes three distinct classifications as noted below.

Low-band 5G Internet of Things (IoT). Low-band 5G uses a similar frequency range to 4G cellphones, 600–850MHz, delivering download speeds a little higher than 4G: 30–250Mbps. Low-band cell towers have a range and coverage area similar to 4G towers. In this range, packaging can be similar.

Mid-band 5G sub-6. Mid-band 5G sub-6 is an upgrade of 4G technology and involves incremental innovation in packaging. Operating at frequencies below 6GHz, the minor modifications of current RF packaging architectures result in minimal changes to the bill of materials (BOM).

5G millimeter Wave (mmWave). 5G mmWave technology is a disruptive innovation. The introduction of mmWave frequencies greater than 24GHz provides opportunities for the adoption of new packaging architectures and platforms. An example is the integration of the antenna into the package. To do this, major design changes and new low-loss materials are required.

5G technology enables advancements in products in all the major integrated circuit (IC) market segments, including: 1) Mobility; 2) IoT; 3) Automotive (advanced driver assistance systems (ADAS)); 4) High-performance computing (HPC)/networking; and 5) 5G network topologies. 5G is more than a new generation of technologies. It denotes a new era in which connectivity will become increasingly fluid and flexible. 5G networks will adapt to applications and performance and will be tailored precisely to the needs of the user.

For 5G, small cells are low-powered cellular radio access nodes that operate in licensed and unlicensed spectrums that have a range of 10 meters to a few kilometers. Small cells are critical to 5G networks because 5G radio waves cannot travel long distances due to 5G's higher frequencies [1].

In a technique called beamforming, the base station computer will continuously calculate the best route for radio waves to reach each wireless device and organize multiple antennas to work together as phased arrays to create beams of millimeter waves to reach the device [2].

Edge computing occurs by locating servers closer to the ultimate user. This distributed computing reduces latency and data traffic congestion. For the 5G ecosystem, cloud data centers provide the computing core. **Figure 1** shows the architecture of these mmWave-enabled changes.

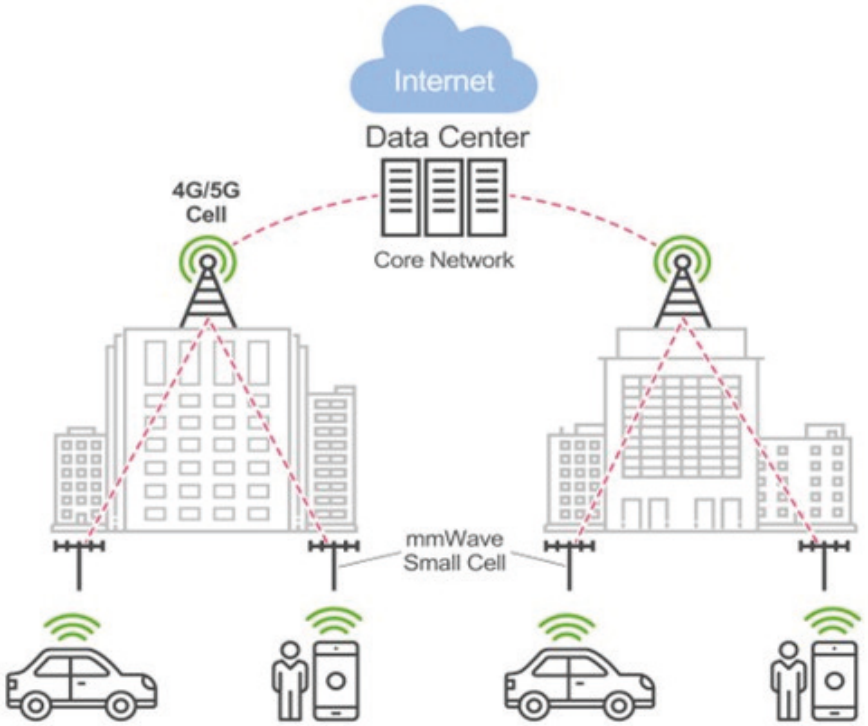

Figure 1: Small cells connected by beamforming technology link to data centers in 5G-enabled communications.

Outlook on 5G market growth

By 2025, 5G networks are likely to cover one-third of the world's population. The impact on the mobile industry and its customers will be profound [1]. In addition, by 2026, 5G will have more than 3.5 billion subscriptions and will grow faster than 4G in most regions, per the Ericsson Mobility Report, June 2021 [3].

The advanced packaging market for 5G RFFEM is projected to reach US$2.3 billion by 2026, representing a 30% compound annual growth rate (CAGR) according to Yole Développement (Yole), SA, an industry consulting firm [4].

"There has been a change in frequencies with the arrival of 5G, adding frequency bands above 3GHz in FR1, and mmWave in FR2," according to Antoine Bonnabel, Technology & Market Analyst, RF Devices and Technology at Yole [5]. "This and the system-level trend have had a profound impact on both the number of components and the technology platforms on which they are built."

RF front-end integration history

The next sections discuss the challenges associated with 5G packaging along with the associated "toolbox" available to enable solutions.

5G IC packaging challenges. Advanced packaging for 5G systems requires the integration of RF, analog, and digital functions along with passives and other system components into a single module. Called heterogeneous integration (HI), the advanced SiP designs that accomplish this integration become more important for 5G because of several reasons, including:

a) Integration of antennas with transceiver ICs and other circuitry;
b) Addition of the sub-6GHz frequency range 1 (FR1) in the near-term through advances in packaging technologies;
c) New mmWave bands frequency range 2 (FR2) drive the integration of RF circuitry, including filters, diplexers, broadband power amplifiers and switches; and
d) The add-on modules to the existing RFFE require optimum miniaturization and component integration.

Further reduction of package size and losses requires close proximity of the transceiver and front-end module. Package-level integration of antennas or antenna in package (AiP) designs within the RF module as well as simultaneous modeling of heat dissipation to keep active components within acceptable thermal limits address these needs. The integration of power amplifiers with antenna arrays to address the design issues of size, cost and performance is a critical step. For package designers, the solution to these challenges incorporates multi-layer fabrication with fine-line features and precise layer-to-layer registration, advanced low-loss materials to reduce conductive losses and co-simulation of circuit, device, package and thermal performance.

The transition to 3D package integration at higher power levels and frequencies requires exceptional isolation between the various circuit blocks. In addition, for high-volume deployment, the manufacturing costs of high-power amplifiers and large antenna arrays in millions of base stations must be addressed [6].

5G RF packaging technology toolbox. To meet the technical demands for complex 5G RF front-end modules, advanced package integration techniques must be deployed. An advanced SiP technology toolbox addresses these demands. Figure 2 identifies the key attributes of an effective 5G technology toolbox.

The growing number of new frequencies, combined with the variety of multiplexing methods, significantly increases the complexity of the RF front-end. Integration using SiP methodology enables customers to design, tune and test RF sub-systems, allowing for a reduction in design iterations and an accelerated time-to-market.

Advanced SiP package integration is being utilized for 5G packaging for a myriad of reasons [7]:

- More flexibility for system designers – to mix and match IC technologies, optimize performance of each functional block and reduce cost.
- Faster time to market (compared to the system on chip (SoC) approach).
- Reduced motherboard complexity – by migrating signal routing complexity to the package substrate.
- Better performance – various ICs and passives placed close together means shorter line length, which reduces resistor (R), inductor (L) and capacitor (C) losses leading to higher signal integrity and lower power consumption.
- Lower system cost – compared to discrete packages, optimized SiP solutions result in overall system cost reduction.
- Small form factor – sub-system size is reduced by integrating multiple dies and passives into a single SiP.
- Improved reliability – better solder joint connections compared to discrete components assembled on a board/printed circuit board (PCB) result because the SiPs are molded, which alleviates stress in the joints.

Figure 2: An advanced RF packaging technology toolbox incorporates many different tools.

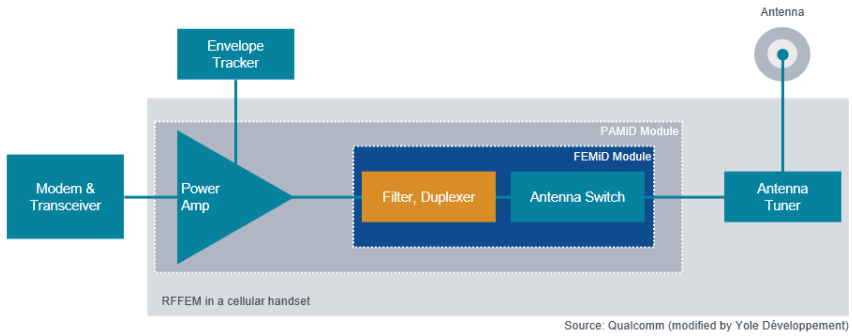

Figure 3: Integrated FEMiD and PA in the cellular handset PAMiD. IMAGE SOURCE: Yole Développement SA.

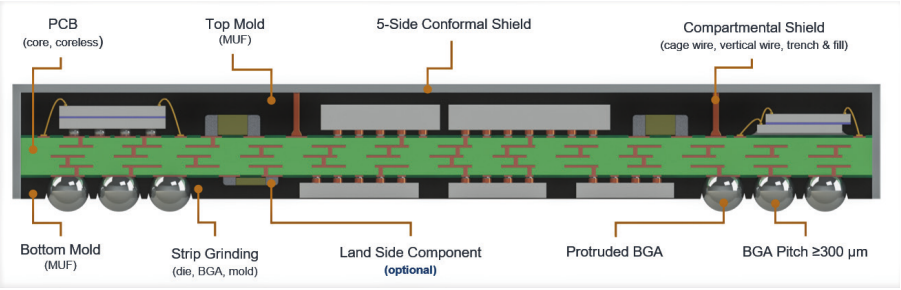

Figure 4: DSMBGA enabling technologies include both top and bottom molded underfill.

The introduction of DSMBGA

To meet the high levels of integration required for 5G front-end modules, an extension of existing single-sided SiP package technologies was pursued. The combination of several enabling package features and assembly processes resulted in the double-sided molded ball grid array (DSMBGA) package. Package development began in 2018 and the first product was released to production in May 2020. **Figure 3** shows a typical block diagram of a DSMBGA front-end module with integrated duplexer (FEMiD) and a power amplifier module with integrated duplexer (PAMiD).

To provide the high level of integration noted above, several enabling technologies were combined to create a DSMBGA front-end module. By utilizing strip grinding, molded underfill (MUF) and double-sided molding, combined with industry-leading design rules, significant advancements in package size reduction were achieved. Other improvements include state-of-the-art conformal and compartmental shielding for electromagnetic interference (EMI) isolation and attenuation and implementation of in-line RF testing to deliver robust and cost-effective assembly technology. **Figure 4** illustrates the extensive technologies applied to create this RF front-end package with key performance attributes. With additional power amplification and filtering circuitry, the DSMBGA package improves signal integrity and reduces losses, resulting in improved Rx/Tx amplification, which translates into reduced system power requirements.

Advanced SiP design rules

A critical benchmark for any IC package technology is its design rules. For DSMBGA, the most advanced SiP design rules are applied to enable a highly integrated and small form factor package. **Figure 5** illustrates the typical SiP design rule attributes for package miniaturization. The minimum spacing for packages and components is directly related to the substrate supplier's process capability (e.g., for solder mask registration) coupled with the package/component physical tolerances, assembly process robustness and assembly materials used. For example, to prevent component tombstoning, the substrate bond pad geometry, solder paste stencil design and solder paste material all interact

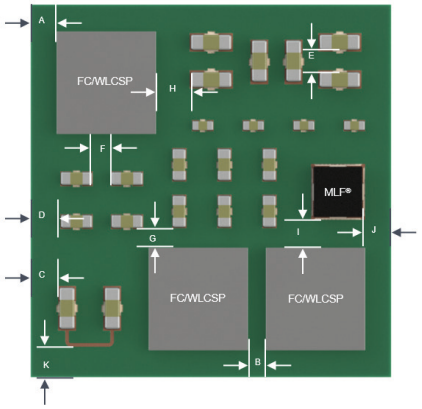

Figure 5: Typical SiP design rule attributes.

and must be optimized for high-volume manufacturing. Molded underfill (MUF) is commonly used to reduce process cost and decrease package spacing requirements. For a robust MUF process, the molding technique (e.g., compression vs. transfer molding), the mold process parameters (e.g., transfer time, pressure, temperature) and the mold compound material must be carefully chosen and optimized to ensure a high-yielding production process. Substrate solder mask thickness control and strategically located solder mask keep-out zones help ensure the molded underfill's process quality and the package's long-term reliability are as robust as possible.

Advanced design rules are rigorously validated through extensive process optimization, workmanship analysis and component/board-level reliability testing. **Figure 6** represents a typical advanced SiP test vehicle (TV) that contains various sized

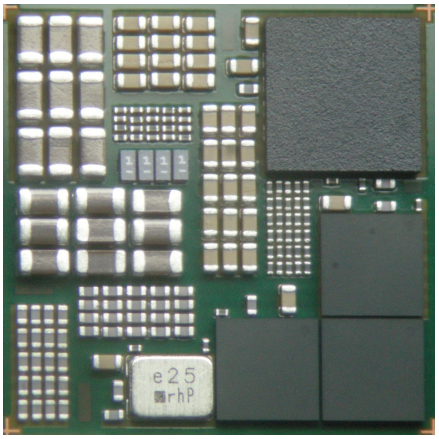

Figure 6: Example of an advanced SiP design rule validation test vehicle.

flip-chip chip-scale packages (CSPs) and passive components. Solder mask-defined and non-solder mask-defined bond pads are incorporated into the TV to validate the effect on component/package stand-off, tombstoning and MUF performance. The assembled test vehicle is then subjected to the typical battery of component-level reliability tests, including high-temperature storage (HTS), preconditioning, temperature cycling (TC), and unbiased highly accelerated stress test (uHAST). Board-level reliability is also verified through temperature cycling and drop shock testing.

EMI shielding

Maintaining signal integrity within the DSMBGA package was essential to guarantee system performance. To minimize any electrical disturbances and resulting signal degradation in an IC and its surrounding circuitry, innovative electromagnetic interference/radio frequency interference (EMI/RFI) shielding needed to be integrated in the structure. **Figure 7** illustrates some of the EMI shielding techniques that have been incorporated into the DSMBGA package.

By leveraging industry-leading physical vapor deposition (PVD) tools, a thin metal stack-up is applied to the external surfaces of the package and coupled to an exposed ground plane in the DSMBGA's organic substrate. This conductive EMI coating is referred to as conformal shielding. By applying state-of-the-art masking techniques, a conformal shield can be applied to select areas of the package, if needed. Compartmental shielding is another EMI suppression technology utilized in the DSMBA package. These compartmental shielding techniques showcase adaptable designs for internal component-to-component shielding with in-package partitioning.

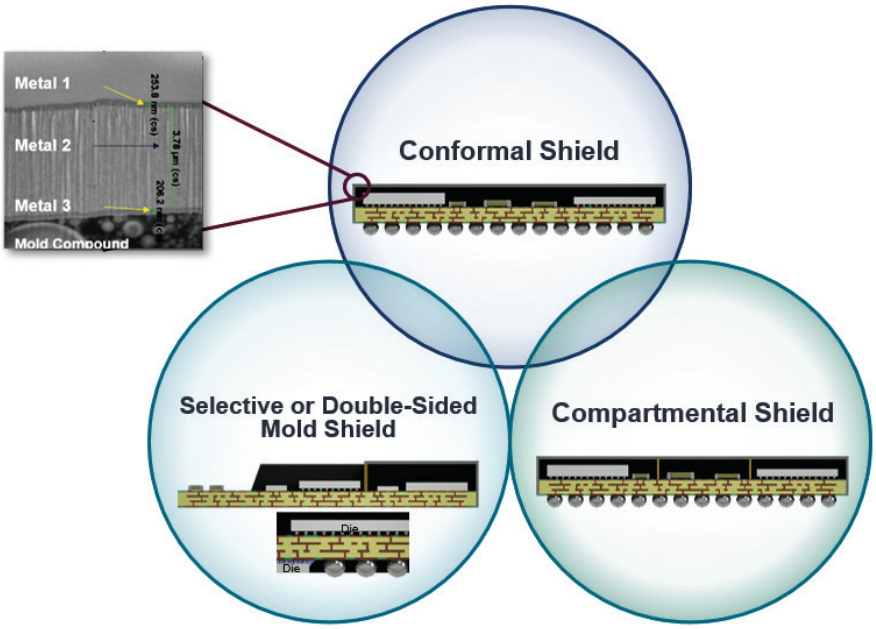

Figure 7: EMI/RFI shielding techniques minimize electrical disturbances in and near the package.

The original compartmental shielding technique was known as trench and fill. Laser ablation was used to create a trench within the mold compound to reveal ground connections on the underlying substrate. A conductive epoxy was dispensed in the trench to form an electrically conductive wall to create the EMI shield partitioning needed. More advanced compartmental shielding techniques have been developed that utilize sophisticated wire bond technologies to create a wire fence, a wire cage or a vertical wire structure within the molded package. Strip grind or laser ablation processes are used to reveal the encased wire. Conformal shielding is then applied to create a Faraday cage effect, whereby the wire structure serves to block electric fields and electromagnetic waves [8]. These EMI shielding structures are shown in **Figure 8**.

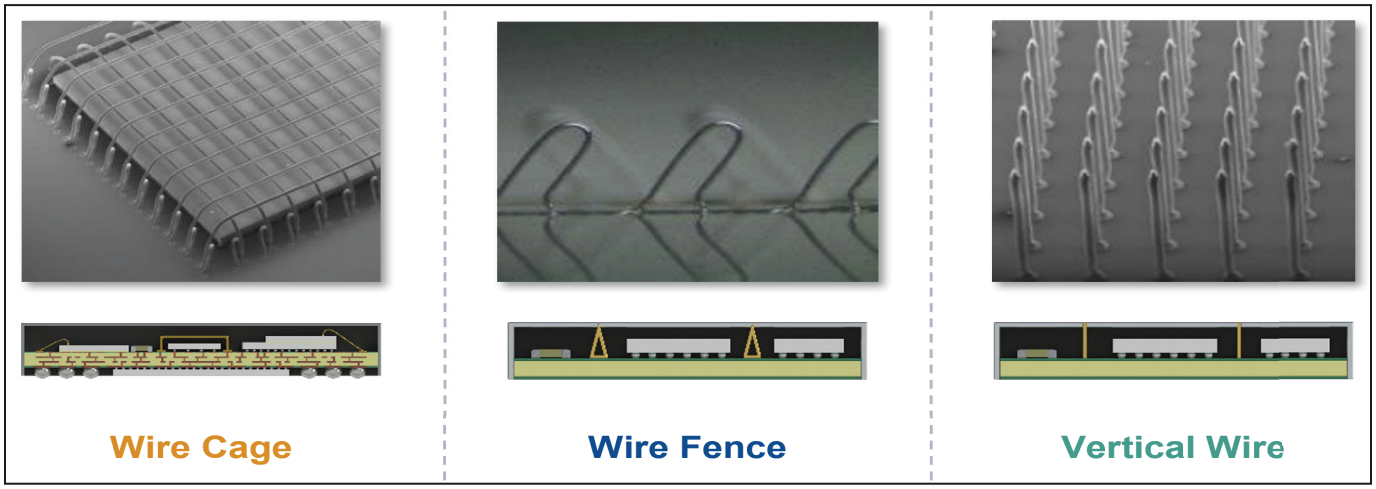

Figure 8: EMI shielding techniques for DSMBGA packages to achieve improved system performance.

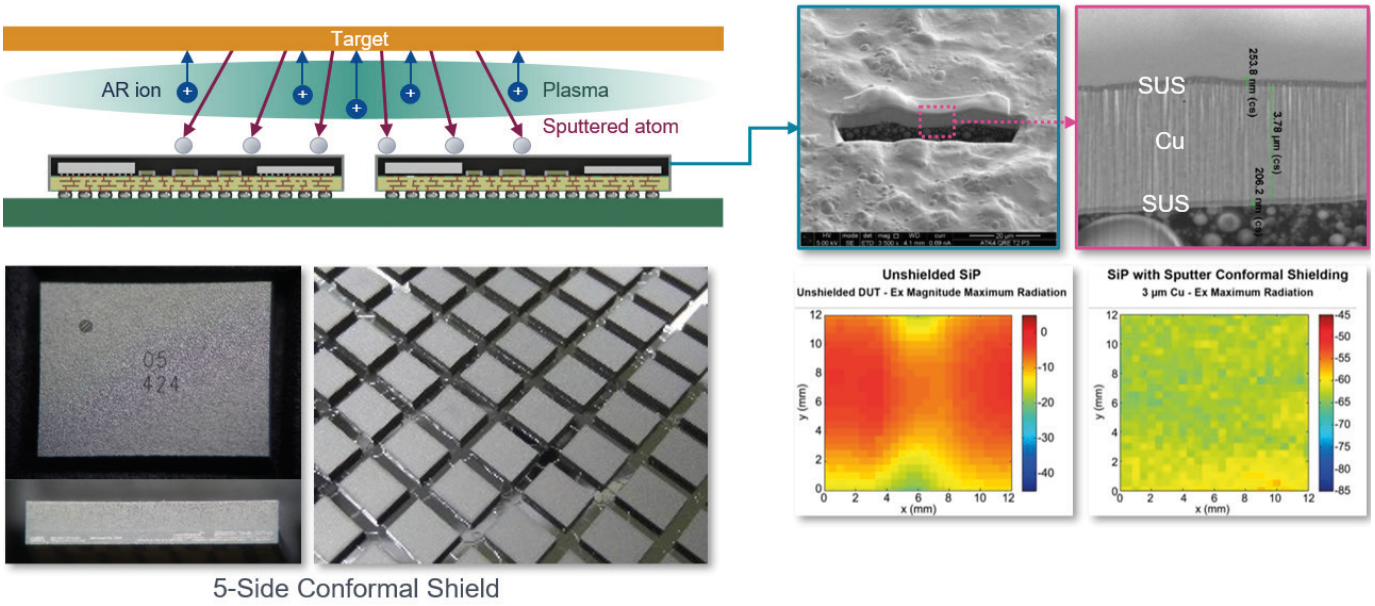

Figure 9: Conformal shielding and EMI radiation suppression effectiveness.

The conformal shielding technology requires strict controls to ensure process quality and yield. To enable this capability, PVD was adapted to package-level processing. **Figure 9** illustrates the PVD conformal shielding technique. A focused ion beam (FIB) cut is used to validate the metal stack thickness. For a 5-sided application, the PVD must be optimized to get accurate and repeatable top surface and sidewall coating to ensure effective EMI shielding. **Figure 9** also compares the EMI shielding effectiveness between an unshielded and a shielded package.

5G front-end module evolution and roadmap

Virtually any 5G RF system circuitry needing component-level integration can benefit from the size, cost and performance benefits offered by the DSMBGA package. The majority of DSMBGA packages being used today are for PAMiD products. Historically, these products were served by single-sided SiP designs because the front-end module circuit complexity was not very demanding (e.g., for 3G applications).

With the advent of 4G LTE, medium- and high-band power amplification and filtering circuity became more demanding with up to five RF front-end modules required

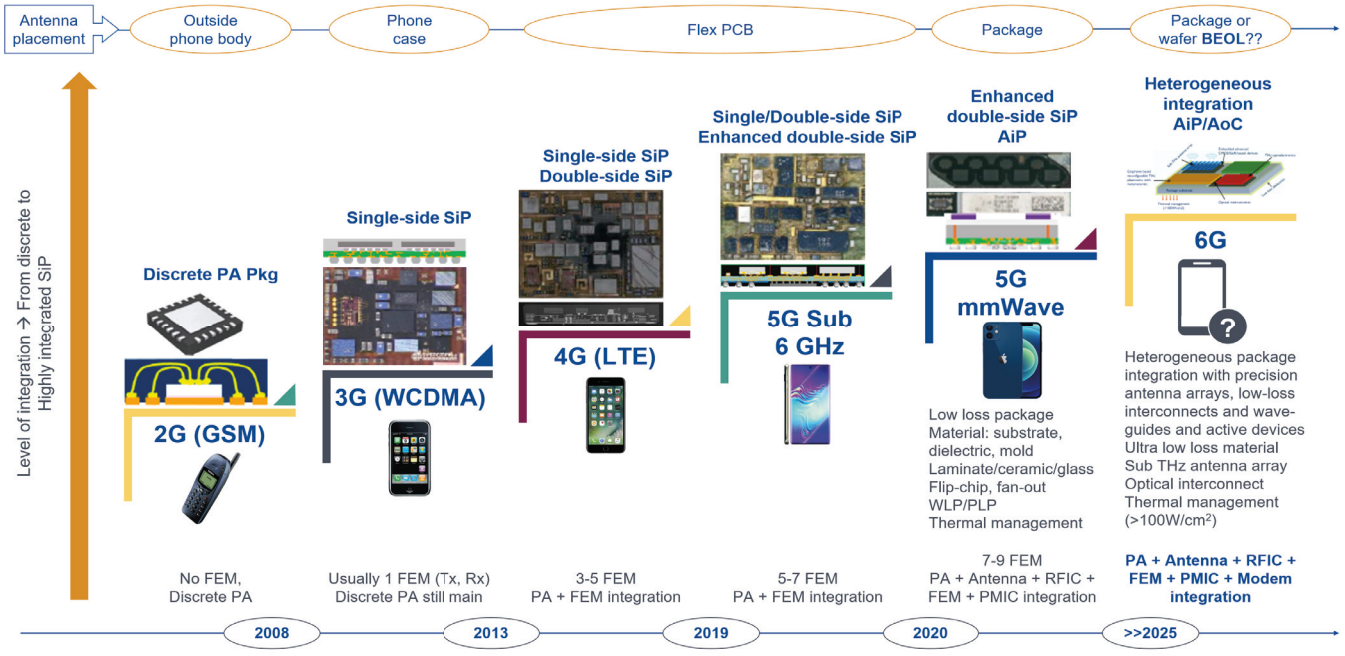

Figure 10: Packaging integration evolution and trends in smartphones. SOURCE: [9]

Figure 11: Example of a PAMiD DSMBGA product showing layout a) (left) before MUF; b) (middle) top; and c) (right) bottom after MUF and EMI shielding.

in a single handset. This led to the evolution of DSMBGA's predecessor, the DSBGA (double-sided BGA) package where ICs were mounted to the bottom of the structure. This allowed for significant module size reduction for the equivalent circuitry in a single-sided SiP structure. Then, with the evolution of the 5G cellular spectrum, front-end module complexity further increased with the introduction of ultra-wideband (UWB) circuitry.

To support these multiple bands, up to seven and nine front-end modules were required for 5G sub-6GHz and 5G mmWave applications, respectively. This resulted in the advent of the DSMBGA package. The latest version of the DSMBGA package is almost 50% smaller than the first mid-/high-band PAMiD. Thanks to innovations such as EMI shielding, flip-chip PA and double-sided molded BGA packaging, PAMiD suppliers managed to integrate the same system in a smaller footprint [9]. **Figure 10** illustrates the evolution and roadmap for RF front-end module integration for 5G smartphones. **Figure 11** shows an example 5G PAMiD product in a DSMBGA package.

Summary

The advanced SiP double-sided molded BGA platform has become an industry technology standard in this domain. Applying leading-edge design rules for 3D component placement and double-sided molding, together with conformal and compartmental shielding and in-line RF testing, delivers integration levels in a small form factor with high yield.

In addition to formidable SiP capacity and DSMBGA technology, an extensive toolset has been developed to maximize performance and to address the sophisticated packaging formats required to productize 5G applications. Some of these tools include AiP, substrate-embedded die, wafer-level SiP and a variety of RF shielding design options. This toolset, combined with expertise in RF module design, characterization and bench test, enables us to serve customers who want to outsource the challenges (including the substantial investment) associated with combining multiple ICs with advanced package assembly and test technologies for 5G networks.

As demand for packages that support 5G climbs, we are well underway with the successful implementation of DSMBGA technology having been in production for high-volume markets for more than a year.

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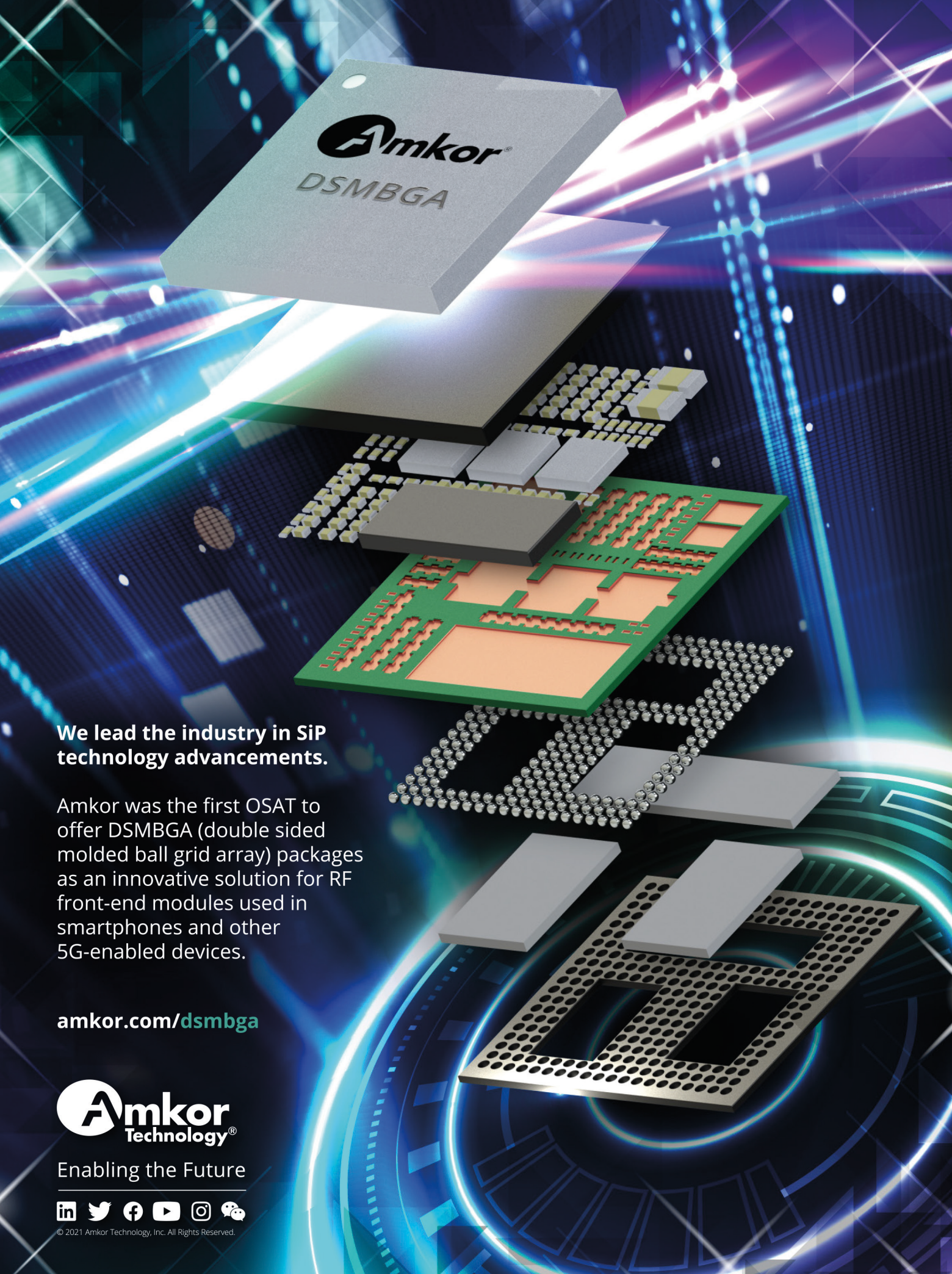
Biography

Curtis Zwenger is VP, Advanced SiP Product Development, at Amkor Technology, Inc., Tempe, AZ. He has held leadership roles in developing Amkor's fine-pitch copper pillar, through-mold via and wafer-level packaging technologies. He is currently responsible for advanced SiP, MEMS/sensor and memory product development. He has been issued 30 U.S. patents and holds a degree in Mechanical Engineering from Colorado State U. and an MBA from the U. of Phoenix. Email curtis.zwenger@amkor.com



We lead the industry in SiP technology advancements.

Amkor was the first OSAT to offer DSMBGA (double sided molded ball grid array) packages as an innovative solution for RF front-end modules used in smartphones and other 5G-enabled devices.

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