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The Future of Semiconductor Packaging

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Enabling AI with heterogeneous integration

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Chip-scale power transistor packaging

By Shaun Bowers [Amkor Technology, Inc.]

Expanding applications for advanced power packaging have created the need for new package design concepts to fill the gaps between existing discrete and power module designs. The integrated power market continues to expand and evolve with established and advanced power semiconductor technologies. Understanding the current environment and the challenges of moving forward are necessary to embrace a new integrated power packaging technology.

The evolving power electronics market

Telecom, data centers, electric and hybrid electric vehicles, and wireless power are among the current applications driving advanced power electronic designs. The global data center power market alone is expected to grow at a compound annual growth rate of 12% from 2019 to 2025 to reach approximately $1 billion by the end of that period [1]. However, DC-DC conversion, DC-AC conversion and simple power switches are required for all electronic products. Improving power electronics in today's designs requires:

- Lower resistance/inductance;
- Integrated controller/logic/passive components; and
- Reduced form factor.

Low on resistance ($R_{DS(on)}$), as well as low inductance (L_{DS}), are necessary to achieve low switching losses in power circuits. Without proper attention to these design details, the package must handle even greater power losses or address lower power application because its power capabilities are restricted. Integrating the controller has become more common with the availability of numerous power control integrated circuits (ICs). Available space in any end design is always at a premium, so a reduced form factor is a must.

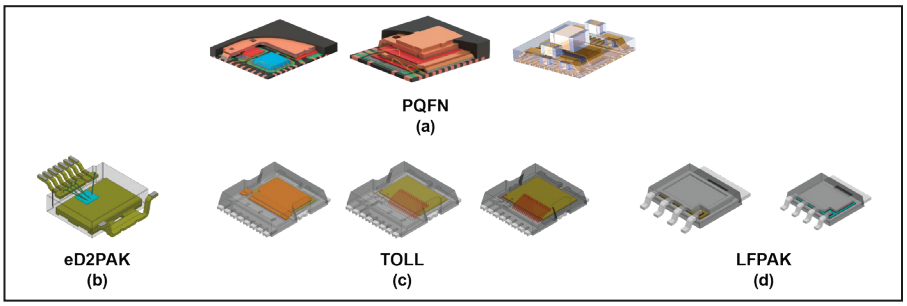

Figure 1: Available power discrete capabilities include: a) PQFN evolution, b) eD2PAK with heat spreader tab, c) TOLL variations, and d) LFPAK.

To address increasingly tougher system design goals, power discrete packaging has progressed from through-hole to surface mount devices (SMDs) with leads, to leadless SMDs, to SMDs with dual-sided cooling and chip-scale metal-oxide-semiconductor field-effect transistors (MOSFETs). Current options to address these requirements include power quad flat no-lead (PQFN), routable lead frame and a host of discrete solutions including exposed double-decawatt package (eD2PAK), TO-leadless package (TOLL) and loss-free package (LFPAK). **Figure 1** shows examples of existing discrete power packaging and the evolution of PQFN packaging. **Table 1** shows a comparison of different characteristics of these packages.

Pkg Type	Pkg Size (mm)			mm²	
	x	y	h	Area	Total Copper Volume %
eD2PAK	14	11.7	3.6	163.8	28.96%
D2PAK	10	10.5	4.45	105	23.24%
TOLL Wire	9.9	10.4	2.3	102.96	17.23%
TOLL Clip	9.9	10.4	2.3	102.96	20.10%
PQFN	5	6	0.83	30	13.65%
LFPAK-BL	4.9	4	1.05	19.6	32.07%

Table 1: Comparative data on existing power packages.

Wide-bandgap (WBG) semiconductor technologies, such as silicon carbide (SiC) and gallium nitride (GaN), have a higher figure of merit (FOM) compared to silicon MOSFETs and have extended the efficiency, output power and/or switching frequency range and operating temperature range for power electronics. At the same time, they have created new challenges and opportunities for power packages.

With lower losses, a given size power device can control higher power loads. For example, with GaN power transistors, a power system can have ¼ the size, weight and efficiency losses compared to a silicon-based system. GaN technology can solve the system challenges from the low-power (50W) end to medium- and even high-power levels in wireless systems and more. Its acceptance in 5G applications makes it well-positioned for sophisticated low- to medium-power packaging. Similarly, SiC has power control capabilities beyond those of Si MOSFETs and requires advanced packaging for many applications. The gains and advantages in WBG devices need new packaging options to maximize the value of the entire power system.

Industry standards are among the ongoing developments that can accelerate the adoption of SiC/GaN power technologies. This is the focus of the JEDEC Solid State Technology Association's JC-70 committee that was started in 2017. With the recent publication of JEP180, "Guideline for switching reliability evaluation procedures for gallium nitride power conversion devices [2]," to ensure the

inherent robustness of GaN devices in power conversion applications, the interest in innovative packaging should increase. An ongoing discussion of JC-70 with automotive-related organizations is also in progress.

Similarly, the JC-70.2 subcommittee is determining guidelines for the testing and reliability of SiC power devices. Both efforts should incentivize and simplify the adoption of these advanced semiconductor technologies, especially if packaging advancements match the semiconductor's capabilities.

Current packaging technology gaps

Today's discrete power packages are limited to the electrical performance of clip, wire and solder interfaces. In general, discrete packaging follows the design philosophy that greater size/volume correlates to higher power handling capability. However, more efficient transistor technology (such as GaN and SiC) provides the ability to handle more power in the same size package or to reduce the form factor significantly.

A PQFN can handle multiple die where power MOSFETs can be stacked or side by side within the same package. To further reduce printed circuit board (PCB) space and improve electrical efficiency, inductors and passive devices can be integrated within or on top of the package.

An ongoing challenge that discrete power packaging and PQFNs encounter is the difficulty to effectively integrate a package size that handles the power required for the application with an adequate interface to address the heat dissipation. A large form factor (LFF) PQFN can have exposed pads for passive integration but is constrained in the I/O density and Cu thickness of the lead frame. A LFF PQFN achieves its capabilities with the tradeoffs of thermal capacity and the increased process complexity of many die attach steps.

For the highest power requirements in applications handling hundreds and even thousands of watts, power is packaged in power modules and package dimensions shift from millimeters to centimeters. These packages are normally attached to large heat sinks with bolts and nuts, and electrical connections are made with large size wires or cables attached with screws.

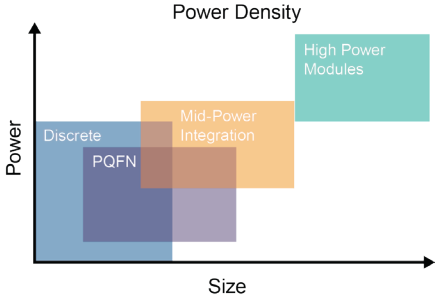

Figure 2: Low- to mid-range power applications provide opportunities for innovative integrated power packaging that overlaps the discrete and PQFN spaces.

These high-power modules may even be water cooled at the system level. As Figure 2 shows, this leaves a gap in the low- to medium-power range that is not filled by either discrete devices or large power modules. This space is ripe for innovation and optimization.

Previous attempts to bridge the gap with embedded technologies have resulted in highly complex designs that were vulnerable to low yield issues, but they did address specific application needs. While many can be considered technical successes, especially to address the niche markets they targeted, their adoption has been limited. With a supply chain mostly enabled through substrate manufacturers, the ownership of yield as well as cost responsibility hindered their adoption and ability to transition to a mainstream power packaging technology.

Ultimately, the need to increase power to package density by removing lossy interfaces has created an opportunity window for a new integrated power packaging concept for low- to mid-range power applications.

A new design concept

To radically improve functionality in the integrated power space discussed above, three things must occur. First, the total conductivity from source and drain needs to be maximized. Second, thermal and electrical interfaces need to be eliminated or considerably reduced in length/thickness. Third, the conductive material density of the package needs to be increased. Reimagining or reinventing the chip-scale package (CSP) for power applications, PowerCSP™ (PCSP) technology accomplishes all three of these objectives, while at the same time reducing the overall size of the device. Figure 3 shows key aspects of this package design including heat spreader (HS) and other options.

To maximize the total conductivity in traditional power packaging, the source and drain need to be connected to current carrying materials at or near 100% of the available space in the die design. Traditionally, this is done by increasing the number of wires, increasing the wire diameter or maximizing the size of the clip attached to the source or drain. In the PowerCSP technology, designs allow the die to use all the available source and drain area by connecting the die directly through a Cu pad that serves both as the current-carrying and heat-dissipating element. Figure 4 shows connectivity options.

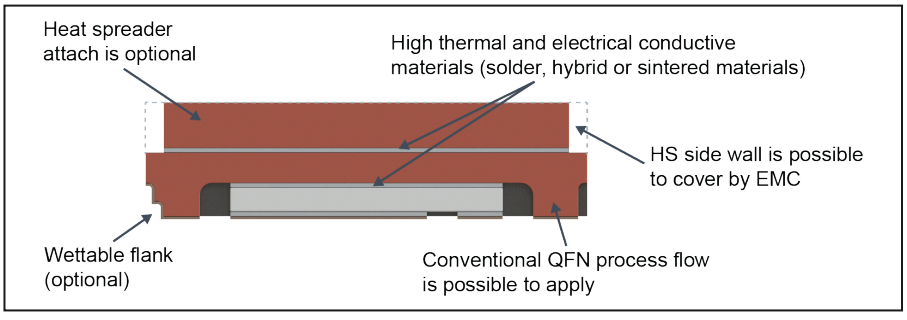

Figure 3: The first implementation of PowerCSP™ technology shows its flexibility and many construction options.

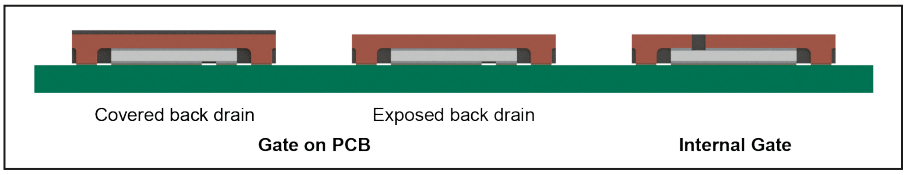

Figure 4: The PowerCSP™ design provides many connectivity options for chip-scale power.

Figure 5: Packaging variations for chip-scale power based on the flexibility of the PowerCSP™ design.

Each interface in a power device can act as a thermal or electrical throttle or an opportunity for failure in harsh environments. As a result, the fewer interfaces in the device and the system, the better, and the trend is to eliminate them to provide a predictable electrical path. PCSP technology minimizes the interfaces to a single connection from the die to the current-carrying element and allows for either the source or drain to be directly connected to the supply or signals in a PCB or other substrate.

To maximize both the thermal and electrical properties, it would be preferred to have as much conductive material as possible within the volume of the package. In most power packaging today, the conductive material in the package rarely goes above 25% (refer to **Table 1**), whereas our new technology is typically in the 40-70% range. This increase is due to the use of a continuous Cu substrate instead of a clip.

There are many tailor-made power packaging designs to address specific needs in the market, but a flexible design that accepts many of the vertical and horizontal MOSFET designs in use today is needed to ensure wide adoption. PCSP variations can utilize the core concepts to address individual application needs while maintaining a high power density. Whether the design involves an exposed source and gate or a routed gate internal to the package, all designs using the new technology achieve a high power density, high conductive material density, and minimal interfaces. Variations also might include additional thickness heat sinks, single- or dual-sided drain designs and the use of solder, sintered, or hybrid materials as needed for individual device performance. Application-specific enhancements like wettable flanks are also possible where needed. The overall size of this new concept can be adjusted to individual die sizes or use common industry footprints. **Figure 5** shows some possible variations.

Whether it is Si, GaN or SiC technology, one of the issues in all semiconductor power devices is higher operating temperatures. Automotive represents the worst case, where under hood operation could require power devices to operate at temperatures of 175°C to 200°C. Packaging is an integral part of addressing the high-temperature challenge.

To achieve a small form factor, one of the tradeoffs of PCSP design is a limited amount of copper in the package in the lateral direction. Even though the new technology uses a thick lead frame above the die, the package mass and size are greatly reduced because of the small form factor. This reduces its integral thermal capacity and requires external heat sinking to achieve an acceptable thermal solution in some applications. **Figure 6** shows the relative junction temperature and mass of various packages modeled when the package is solely responsible for thermal dissipation. If the heat sinking is available or easily added, this limitation is easily resolved.

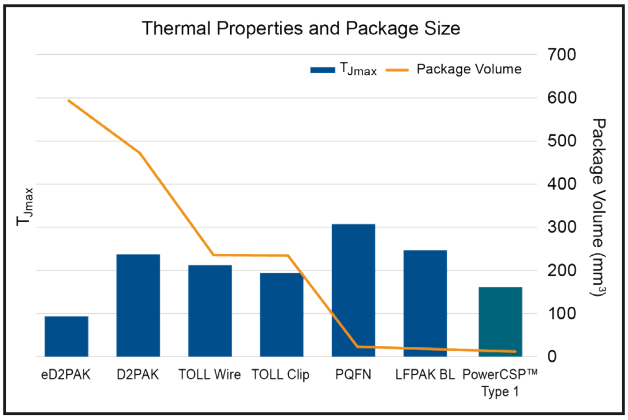

Figure 6: Relative junction temperature vs. package volume for various power packages.

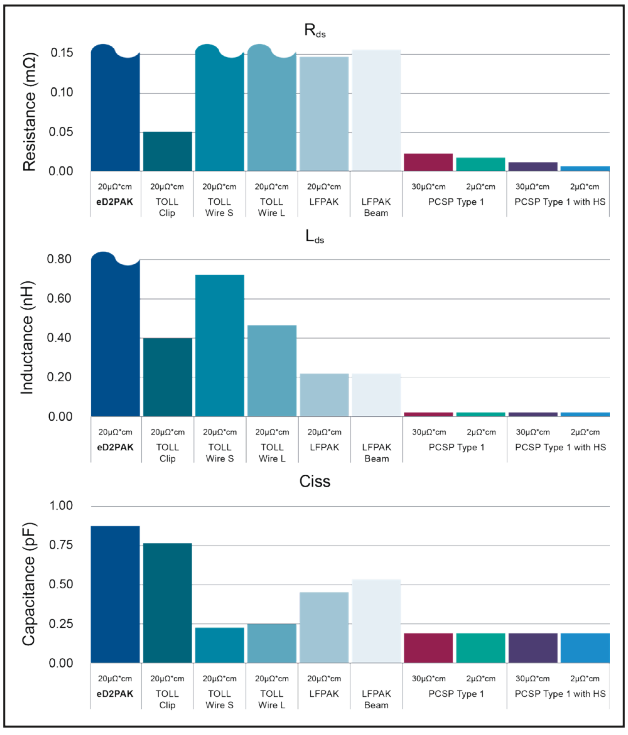

Figure 7: Simulated comparison of R_{DS}, L_{DS} and C_{iss} for the PowerCSP™ (PCSP) design to different versions of eD2PAK, TOLL and LFPAK packages.

Each of the design variations will still utilize the refined process to manufacture high-density power devices that are already well-established. Eliminating the need for wires and/or clips removes process steps in the manufacturing flow compared to traditional power packaging. For the PCSP design, the frame is the electrical clip, so 2-3 process steps are avoided in the manufacturing process. The key process steps are die attach, mold and singulation, whereas other package variants might have additional steps like wire bond, solder printing, clip placement, and an additional cleaning step.

The result of the PCSP design elements allows low resistance (R), low inductance (L) and good capacitive (C) performance compared to other discrete packages. **Figure 7** shows the modeled RLC of the package against other discrete power packages (refer to **Figure 1**) and with different interface materials for the die to body connection. The results are predictable for a package with a very high density of conductive

material. Resistance is very low compared to other packages because of the large conductive interface and direct connection to the PCB. The inductance is low for the same reasons and capacitance is slightly lower than other packages. The RLC performance does not appear heavily dependent on the conductivity of the die attach material or thickness of the new design itself, although this will benefit thermal and maximum current delivery from a basic point of view. Loss density is very low compared to devices using wires. The electrical simulation validates the performance of the design compared to both smaller and much larger packages.

Low- to mid-power integration using the PCSP concept

There is a strong movement towards integration within the power market—and power density plays a big part in the adoption of various integration methods. In the low- to mid-power range, integration can involve different methods depending on the use case and the original package format.

Three basic approaches outline different paths to integration. One is to simply include the controller and MOSFET devices into a split-pad lead frame, or PQFN. This is common, but limited as far as power and performance are concerned and options to add passive elements are typically done off-package. Another is to include more exotic materials within the molded interface such as direct bonded copper (DBC), which is common in insulated-gate bipolar transistor (IGBT) modules. Last, there are efforts to directly embed the MOSFET dice into a laminate substrate or redistribution layer (RDL) package. Although the embedded option has merit in mid-power options, supply chain issues have historically slowed widespread adoption of a fully-embedded option. Each of these integration paths has advantages and disadvantages, but share a few common traits. They all attempt to maximize the contact area to the source and drain of the FET, put as much conductive material as possible within the module, and design a reduced electrical path for successful integration.

An approach to integration that uses PCSP technology might resolve some of the fundamental issues inherent in the other approaches. Starting with a common form factor and integrating this approach into more mainstream module aspects will allow for wider adoption. Allowing the MOSFET(s) to be pre-packaged allows for individual or gang testing, therefore it can be treated as known good die (KGD) for improved yield. Mounting a package directly to a substrate and PCB may reduce the overall complexity and cost.

The modular approach should also enhance the performance of the overall system because of some specific design options for the integrated device. Signal paths directly to the PCB will maintain low resistance/inductance. Using a high-density but small form factor package allows thick Cu interfaces only in areas critical to the design. Also, critical components and devices can be distance-optimized for performance and cost. By applying this approach to a typical half-bridge circuit, the advantages of the design freedoms become more obvious. In a half-bridge circuit, one of the critical design aspects that greatly affects performance is the distance from the source of one MOSFET to the drain of another and the inductor. With the use of PCSP design, the inductor can be placed directly between the MOSFETs and the distance can be very short and optimized to minimize line inductance between the MOSFETs and the passive components. **Figure 8** shows this approach.

If further integration is needed, or routing is needed on both sides of the MOSFET, there are simple concepts that can be used as alternatives to embed within substrate technologies. In **Figure 9**, two thin laminate structures are used with a molded MOSFET structure in between. These designs and processes are mature but used in mobile, rather than power, applications. The simplicity and process re-use may make this a valuable alternative in the future because of its maturity and fast time to market.

Low- to mid-power integration innovation

New applications for power electronics in automotive, telecom, data centers, consumer and other areas, as well as advanced power transistor technologies, have created the need for innovative power packaging to fill the gap between existing discrete power packages and power modules in power conversion.

The PCSP design provides a MOSFET CSP that enables a high-power density package. This capability is applicable to SiC and GaN transistors and can be a key building block towards integration. It uses a smaller form factor that is scalable to die size or a standard, high-volume format. The design has the flexibility to address a variety of applications, uses KGD and thick copper only where needed to reduce cost, and provides a reduced electrical path to active/passive elements for increased efficiency and lower noise. A patent has been filed for this design approach.

The low-power market, like smartphones, has already implemented wafer-level CSP MOSFETs. This mounting of a power transistor directly to the mother or a daughterboard is already occurring and could expand with the availability of advanced chip-scale

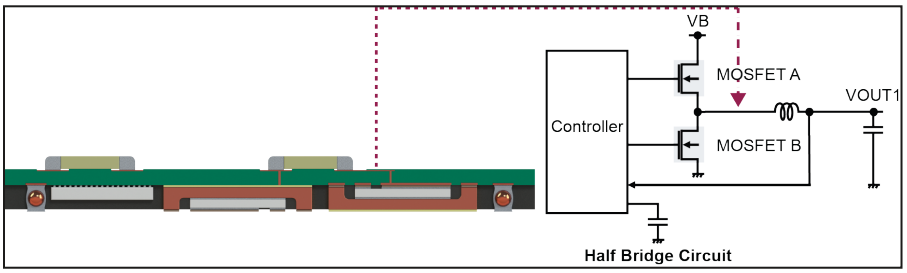

Figure 8: The PowerCSP™ design methodology can be used to construct a power module package.

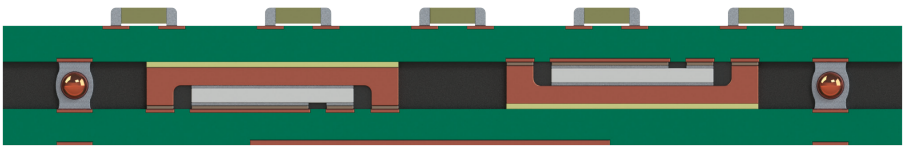

Figure 9: Increased integration of power using the PowerCSP™ methodology.

power packages. With this evidence of surface-mounted packaging in consumer power electronics, the acceptance of a low-noise package in lower power applications should provide a means for our new methodology to extend that design philosophy into higher (medium) power regions.

While integrated device manufacturers (IDMs) typically have their own in-house approach for packaging and use outsourced assembly and test suppliers (OSATS) for special purposes, integrated power could be one of those special purposes that dictates a dedicated OSAT position. This inherent supply chain benefit of OSAT production simply adds to the advantages of the smaller, cooler (with appropriate heat spreader), quieter and cheaper capabilities of our new design approach. Combined, these advantages could lead to widespread adoption of this low-resistance/low-inductance package.

Acknowledgment

PowerCSP is a trademark of Amkor Technology, Inc.

References

1. "Global data center power market size to generate revenues," Arizton Advisory & Intelligence report; https://www.openpr.com/ news/2047478/global-data-center-power-market-size-to-generate-revenues
2. "Guideline for switching reliability evaluation procedures for gallium nitride power conversion devices," JEP180; https://www.jedec.org/standards-documents/docs/jep180

Biography

Shaun Bowers is VP, Mainstream Advanced Package Integration at Amkor Technology, Inc., Tempe, AZ. He joined Amkor in 2000 and is currently responsible for package development in automotive, lead frame and power business segments. He previously held technical program management, sales and customer service roles as well. Prior to joining Amkor, he worked for Johnson Matthey Electronics and Honeywell Electronic Materials. He holds a degree in Mechanical Engineering from Gonzaga U. Email shaun.bowers@amkor.com