Low-Density Fan-Out SiP for Wearables and IoT with Heterogeneous Integration

A. Martins[*], M. Pinheiro[*], A. F. Ferreira[*], R. Almeida[*], F. Matos[*],
J. Oliveira[*], Eoin O´Toole[*], H. M. Santos[†], M. C. Monteiro[‡], H. Gamboa[‡], R. P. Silva[*]

‡Fraunhofer Portugal AICOS, Porto, Portugal
†INESC TEC
*AMKOR Technology Portugal, S.A.
Avenida 1º de Maio 801, 4485-629
Vila do Conde, Portugal

ABSTRACT

The development of Low-Density Fan-Out (LDFO), formerly Wafer Level Fan-Out (WLFO), platforms to encompass the requirements of potential new markets and applications such as the Internet of Things (IoT) is crucial to maintain LDFO as the leading Fan-Out technology. This drives the development of a new set of capabilities in the current standard LDFO process flow to break through the existing technology boundaries.

One of the most widely discussed advantages of LDFO packaging is heterogeneous high-density system integration in a package. LDFO System in Package (LDFO SiP) integrates active dies, passive components and even already-packaged components using other packaging technologies. This heterogeneous integration is based on a wide range of different geometries and materials placed inside the LDFOSiP with high accuracy.

Ultimately, heterogeneous integration will be fundamental to achieve new levels of miniaturization. However, multi-die solutions face several challenges such as bare-die availability, passives integration, antenna integration, low power budget, test complexity and reliability.

Package research and development (R&D) must overcome all of these issues to build a product with high volume manufacturability. The wafer level SiP (WLSiP) technology required to enable the new features and processes needs to be ready for high volume manufacturing of new products at high yield and reasonable cost.

This paper presents the approaches used to effectively enable LDFO SiPs (WLSiPs):

1. A pre-formed vias solution is employed to connect front to back side of the package, including development for high accuracy via bar placement.
2. A wafer front-side to back-side redistribution layer (RDL) alignment solution was developed.
3. Space requirement reduction between components to achieve the smallest possible package.
4. Miniaturized Bluetooth antenna integration in the RDL.
5. Creation of a stacking concept (vertical connections to create a modular system that enables easy addition of new features to the final product).

Inside the package (excluding the area reserved for the antenna), components are densely packed: several sensors, power management components, radio communication and all required passives are incorporated into a single WLSiP. Connecting all these features to create a component that works by connecting only a single battery required implementing a double sided, multi-layer RDL, while maintaining the ability to create a 3D solution by stacking vertical connections for several other solutions. The result is an approach that easily adapts the system to a variety of customers' needs.

The work done is part of the collaborative COMPETE2020-PT2020 funding program under "IoTiP- Internet of Thing in Package" project nº 017763, Projetos de I&DT Empresas em CoPromoção.

Index Terms — LDFO, LDFO SiP, Fan-Out WLP, WLSiP, SiP, Multi-Chip-Package, Antenna-in-Package, Package-on-Package, Through Mold Via, TMV®, TPV

INTRODUCTION

Despite the increasing number of smart devices, there are still many challenges that have a negative impact on the expansion of the Internet of Things (IoT). Advanced packaging will play a major role to resolve these issues, since the technology calls for the integration of microelectromechanical systems (MEMS), sensors, connectivity, memory and processing. Ultimately, SiP technology will be fundamental to achieve new levels of miniaturization.

Low-Density Fan-Out (LDFO), wafer level System in Package (WLSiP), addressing "more than Moore" challenges in system-level miniaturization, is important to meet the increasing demand for innovative products with a smaller form factor, higher performance and increased functionality without compromising manufacturing cost. IoT and wearables are some of the areas where these developments are increasingly valuable.

To fulfill these demands, semiconductor packaging companies have different technologies available. The most common approach is traditional flip chip on laminate substrate but other technologies are emerging such as embedded die in organic laminate and WLSiP [1] [2].

WLSiP combines different electronic components together into a single package with shortest electrical distance, optimizing performance [3], and reducing the amount of traces going into and out of the package, with the potential to simplify final application printed circuit board (PCB) design and cost.

Package-on-Package (PoP) technology integrates multi-chips using 3D stacking of two or more packages and either saves PCB space or avoids the PCB entirely. When used in 3D stacking configuration, LDFO has even greater advantages by achieving thinner packages since it does not use a substrate. Wafer level PoP methods are reported using through package via (TPV) interconnections to connect the top and bottom packages and, in some cases, a back-side redistribution layer (RDL) [4]. TPV can be achieved with different methods, such as PCB via element, vertical interconnect element, through silicon via (TSV) die, laser drilled through via or laser drilled blind via [5].

This paper explains the technical challenges that were encountered with an LDFO process to manufacture an autonomous SiP with 26 components, including Antenna-in-Package and Package-on-Package technology. The chip-first process flow is proposed for a multi-die LDFO SiP with a multi-layer structure. PCB via elements were used to vertically connect the front side RDL and the back side RDL. The back side RDL provides both the shielding and antenna ground plane.

I. System-In-Package

To demonstrate the full potential of the chip first LDFO SiP approach, a test vehicle was proposed that contains all the components required for a fully functional and autonomous system, integrating all active and passive components for sensing, processing, energy management and radio communications, including the Antenna-in-Package.

This SiP will also provide a physical interface, a vertical Bus, to enable a modular architecture, through PoP, for adding new features, such as additional sensors or larger memory that can be of practical use in a variety of applications. The PoP is achieved with TPV (**Figure 1**) interconnections to connect the top and bottom RDLs with the POWER and DATA vertical buses.

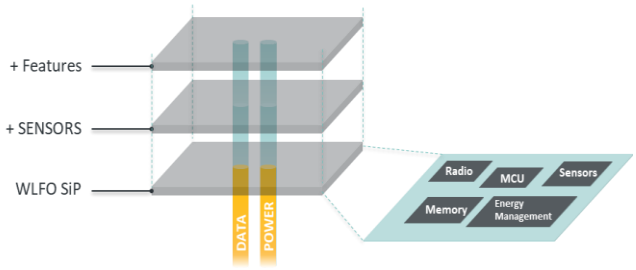


Figure 1. Test vehicle stack concept.

SiP Components

The proposed SiP embeds sensing, processing capabilities, energy management and a Bluetooth Low Energy (BLE) radio, and integrates additional components as shown in Table 1.

Table 1. SiP components and package types including land grid array (LGA) packages.

Component	Package
ARM® Cortex™ M, Flash, RAM and BLE transceiver	Bare-die
3-axis accelerometer & 3-axis gyroscope	LGA
3-axis geomagnetic sensor	Bare-die
2.44GHz Balun	Bare-die
High and Low freq clock sources	LGA
Step Down DC/DC	Bare-die
DC/DC capacitors & inductor	SMD
RF and decoupling capacitors	SMD

The goal is an autonomous SiP that requires just the power supply, either a Li-ion rechargeable battery or a 3V coin cell, to be fully functional. As shown in Figure 2, other signals, besides POWER and DATA vertical buses, are also accessible in smaller pad sizes and are required for final test or for additional functionalities when the SiP is soldered onto a PCB.

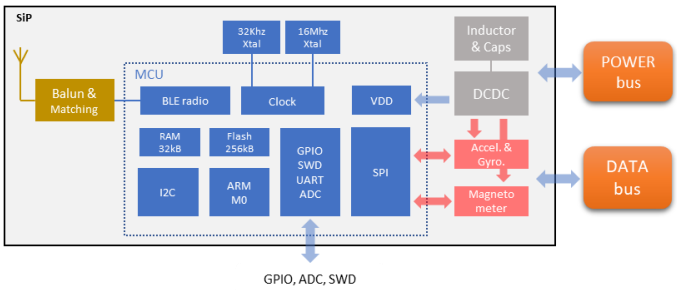


Figure 2. SiP block diagram.

Antenna-In-Package

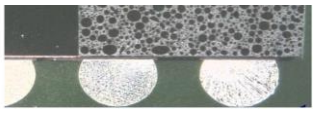
One of the challenges for this SiP was designing an omnidirectional antenna in such a small package. The target was to have a SiP with an antenna that needs no external ground plane to operate. All RF components, including the balun and matching network are embedded in the SiP.

The RDL layout comprises the system area with signal traces and the antenna area. The antenna area is a keep-out zone for routing for both the front and back sides. The back side RDL provides shielding, an antenna ground plane and the pad layout for PoP.

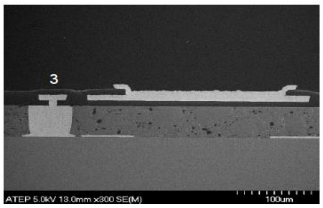
II. LDFO SiP Process

The LDFO technology was chosen based upon the attributes required for SiP construction.

Option 1: Chip first – first dielectric of RDL directly over the die surface:



Option 2: Chip first – dielectric/copper pillars directly over die surface. RDL processed on top of copper pillars:



Option 3: Chip last – RDL processed on carrier and chip is assembled on the RDL.

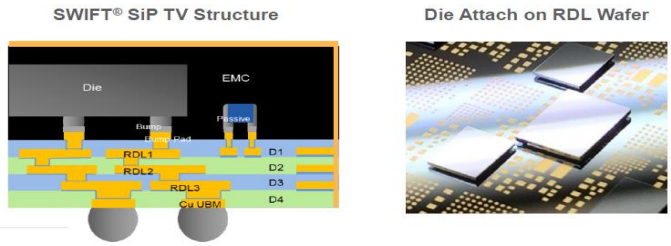


Table 2 shows the decision table for the technology choices.

Table 2. Technology decision matrix.

	Suitability for SiP	Complexity / cost
Chip First RDL direct	+++	+++
Chip First RDL on pillar	-	-
Chip Last RDL on carrier	++	-

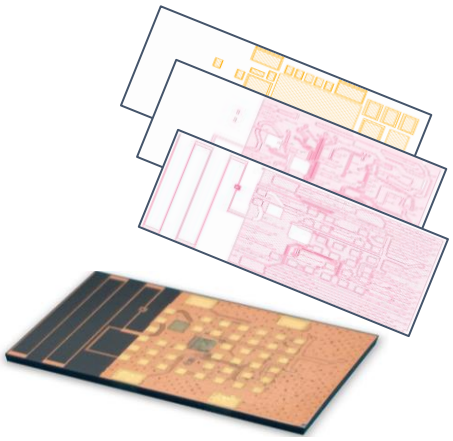
For more complex and expensive dies, the chip last option may be worth considering since the yield associated with applying the expensive die to known good RDL may counter balance the increased process cost.
The technology chosen is the chip first with RDL directly over the die surface.
In this technology, a wafer reconstruction process is employed, where known good die (KGD) and other devices/packages/components are placed side-by-side on a temporary bonding tape. Subsequently, all parts are embedded in epoxy molding compound (EMC) via compression molding, see Figure 3.

Figure 3. LDFO wafer reconstruction process.

This is followed by the RDL process. This consists of spin coating of photoactive dielectric which is patterned and cured and sputtering of a seed layer which enables electroplating after patterning of a plating photoresist. Multiples of these steps as

Figure 4. RDL build up.

required for multiple RDL layers and/or under-bump



metallizations (UBMs).

Leveraging the flexibility of reticle based multi-project design in different positions of the reticle field several additional features were incorporated in the same wafers for process control and for variants. These include:

- Meander structures for leakage current control between RDL in the same structures and for RDL 1 to RDL2 to guarantee the dielectric coverage of the first RDL
- Kelvin structures for die to RDL contact resistance control and for RDL1 to RDL2 contact resistance measurements
- Kelvin structures that permit the measurement of the contact to the individual embedded passive components to validate the quality of the electrical contact to the passive devices

Figure 5 shows the process control monitor (PCM) structures.

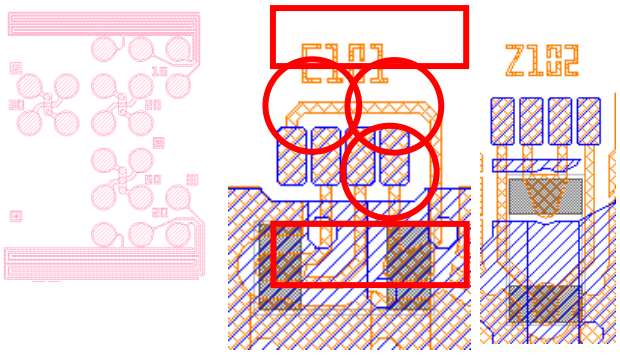


Figure 5. PCM structures

As shown in Figure 6, the RDL layout is divided in two distinct areas: the system area with signal traces (blue area) and the antenna (green area). The area reserved for the antenna is an area without any component routing or any other copper except for the antenna itself.

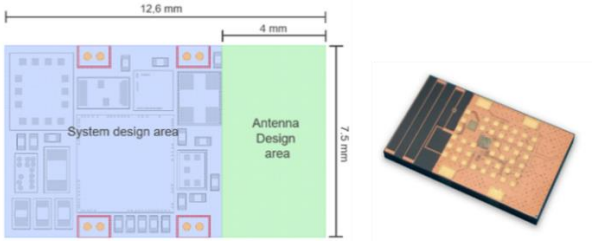


Figure 5. SiP layout.

Included in the multi-project reticle were different antenna variants from the ideal, simplest most cost-effective approach to the most expensive, see Figure 7.

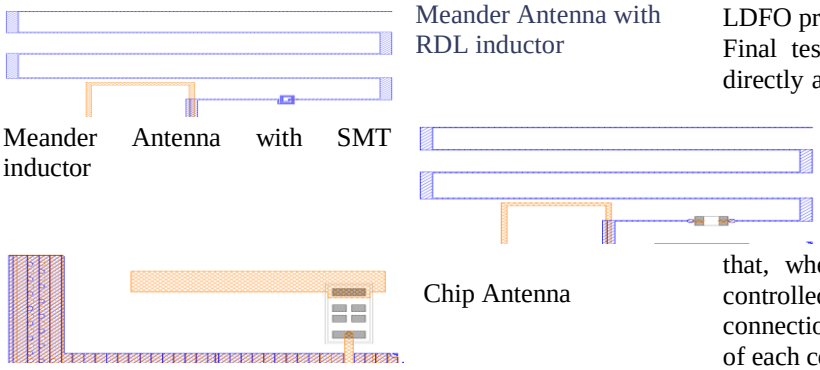


Figure 7: Antenna types in the test vehicle.

To enable a modular architecture for adding new features, such as additional sensors or larger memory, TPV-based in PCB via elements were included to establish the interconnections between the frontside and back side RDLs (see Figure 8).

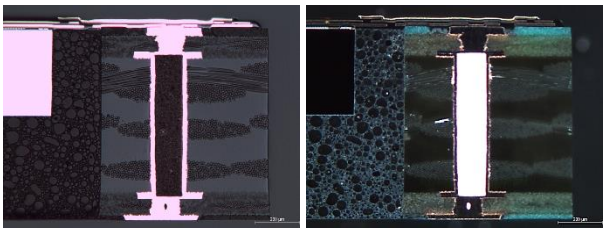
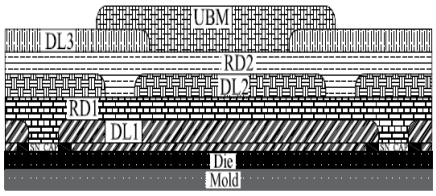


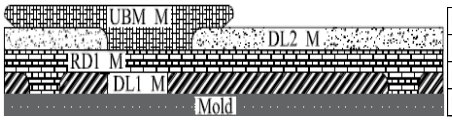
Figure 8: Shared TPV – package's left side (left: brightfield; right: darkfield).

Typical RDL stack-up for the front side of this type of package is:



UBM	10µm
DL3	10µm
RD2	5µm
DL2	10µm
RD1	5µm
DL1	10µm

Typical RDL stack-up for the backside RDL is:



UBM	10µm
DL2	10µm
RD1	5µm
DL1	10µm

The final dimensions of 12.6 mm x 7.5 mm are produced on large diameter, reconstituted wafers.

Final Test

Final test is performed at the component level through direct contact on device pads with a test socket (Figure 9) and relies on the assumption that embedded ICs for sensing, processing, and energy management are assembled as known-good-die or pass components. However, a functional test will verify the RDL interconnections and any damage that could occur during LDFO processing.

Final test contains DC tests performed by DC instruments directly at the SiP pads, such as open/short, leakage and other DC measurements.

Functional tests are performed via Serial Wired Debug (SWD) SiP pads by programming the SiP with test code. Knowledge of the SiP architecture enabled the development of test code (firmware) that, when flashed in the SiP MCU memory, performs a controlled functional test, validating the internal SiP connections between components and the correct functionality of each component per the respective datasheet.

The radio tests, performed with direct contact to the RF SiP pads and SWD pads for test control, validate the SiP RF transceiver, balun and matching network for the BLE channel frequencies. The RF test has two modes of operation: the

transmit test mode, where the device under test generates a predefined set of test packets; and a receive test mode, where the device under test counts the number of test packets received.

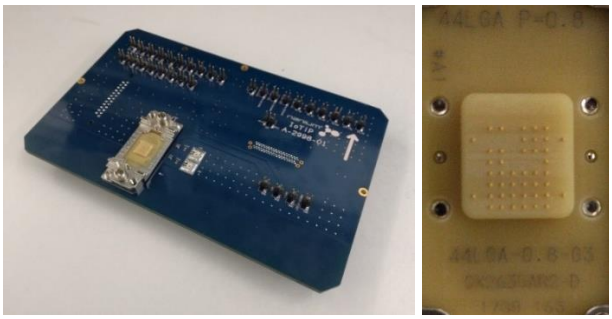


Figure 9. SiP test load-board and socket.

The hardware used at final test, both for automatic and manual handling, includes an in-house design test load-board (Figure 9), rack and stack instruments for contact, leakage and DC tests, bench test instruments for RF tests and a computer for SiP firmware flash and test sequence control.
The previously explained electrical tests with full coverage of all SiP elements were the primary readout method for all reliability testing performed on the test vehicle.

Application Test

Final test is essential to screen design and packaging defects. In the presence of a nonfunctional SiP, the fail signature is important to identify the defective structure.
The application test is performed by a second equipment with BLE radio that used various smartphone models. With the application test firmware programed in the SiP and the correspondent application code in the smartphone, the SiP sensors can be controlled via BLE and sensor data can be acquired and displayed in the smartphone display (Figure 10).
All devices that passed final test were 100% functional in the application test. This served to revalidate the functional test and antenna function.

Figure 10. SiP soldered directly to Li-Ion Battery (left picture) and smartphone reading SiP sensor data via BLE (right picture).

III. Reliability Test Results

For this evaluation, ten fully functional units were submitted to PRECON MSL1, with a subsequent electrical test. After PRECON, two units were removed for later physical characterization and the remaining units were evenly split between Unbiased Highly Accelerated Stress Test (UHAST) and temperature cycling (TC), as shown in **Figure** . These component level tests are standard for mobile electronic devices and are most indicated to stress interfacial adhesion critical for package with heterogeneous integration.
In the case of TC two read-outs were carried out, one after 1000 cycles (JEDEC pass criteria) and the other one after 1500 cycles.

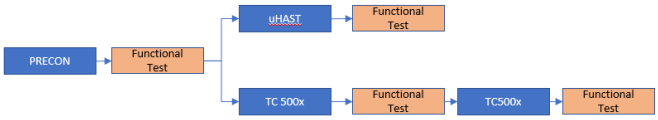


Figure 11. 1st-level reliability flow.

All the assessments were based on the electrical functional tests. A detailed summary of the 1st-level reliability results is presented in Table 3. After the TC 1000x electrical assessment, the units were returned to test to complete 1500 cycles.

Stress	Condition	Pass/Fail Criteria	Status
PRECON (JESD22-A113) (J-STD-020)	MSL1 No thermal cycling Bake: 24h/125ºC Moisture soak: 85ºC/85%RH Reflow T_{peak}: 260ºC (3x)	Functional test 0 Fail	100% PASS
PRECON + uHAST (JESD22-A118)	Condition A 130ºC/85% RH	Functional test 0 Fail/96h	100% PASS
PRECON + TC (JESD22-A104)	Condition B -55ºC↔+125ºC 2 cycle/h	Functional test 1000 cycles	100% PASS
PRECON + TC (JESD22-A104)	Condition B -55ºC↔+125ºC 2 cycle/h	Functional test Non gating/1500 cycles	100% PASS

Table 3 – 1st-level reliability summary.

After the prolonged TC stress, cross sections were performed focusing on interfacial adhesion and on the PCB vias since Moisture Sensitivity Level 1 (MSL1) preconditioning is not typical for PCB materials. Figure 12, 13 and 14 show the results.

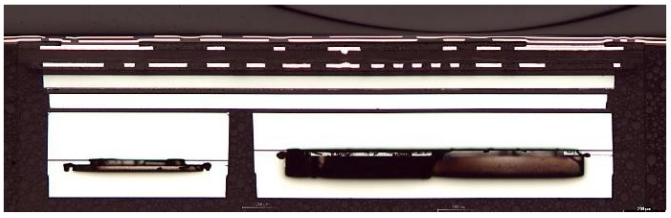


Figure 12. Cross sections of mold to mold interface of pre-molded packages.

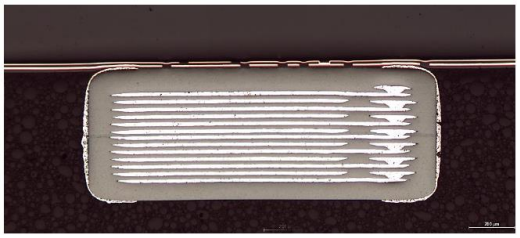


Figure 13. Mold compound adhesion to the surface mount devices (SMDs).

Figure 14. Mold compound adhesion to the PCB vias.

No cracking or delamination of the principle interfaces was observed for mold compound to mold compound, mold compound to die or SMD to mold compound even after extended TC testing. However, PCB via and interface PCB to mold compound were observed as shown in Figure 15.

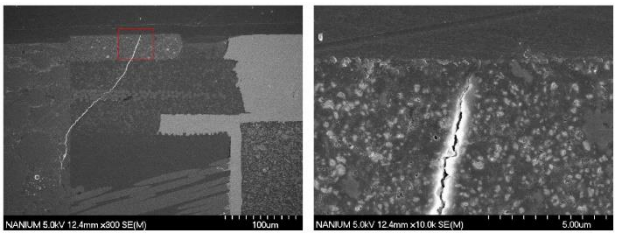


Figure 15. Cracking in the PCB via and interface PCB to mold compound.

IV. CONCLUSION

The development of a LDFO SiP as a standalone solution, integrating a variety of components and materials, was demonstrated based upon die first RDL directly on the die surface. The goals accomplished during this work can be summarized as:

- A miniaturized 2.44 GHz antenna constructed in redistribution layer was designed and characterized. All of the antenna variants were found to be functional.
- A pre-formed via solution was employed to connect front to back side of the package.
- Wafer front-side to back-side RDL alignment solution based on infrared (IR) alignment in the stepper was employed.
- All active and passive components for sensing, processing, energy management and radio communications were integrated.

LDFO SiP process for high volume was demonstrated for a multi-chip, 7.5 x 12.6 mm^2 package with two layers fine pitch RDL connecting 26 components from several packaging types and PCB via elements.
These test vehicles were submitted to 1^{st}-level reliability tests, including Preconditioning MSL1, 1500 x TC, UHAST and high temperature storage (HTS). The results showed electrical pass in all stress tests performed.

ACKNOWLEDGMENT

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