CHIP BOARD INTERACTION ANALYSIS OF 22-NM FULLY DEPELETED SILICON ON INSULATOR (FD-SOI) TECHNOLOGY IN WAFER LEVEL PACKAGING (WLP)

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ABSTRACT

Recently, Wafer Level Packaging (WLP) has been in high demand, especially in mobile device applications as a path to enable miniaturization while maintaining good electrical performance. The relatively inexpensive package cost and simplified supply chain are encouraging other industries to adapt WLP capabilities for radio frequency (RF), communications/sensing (mmWave) and automotive applications. However, to date its application space has been limited to a small die form factor due to challenging chip board interaction (CBI) control. The combination of ultra-low dielectric constant (ULK) based advanced silicon technology and WLP is another challenge for industry to overcome.

In this article, to systematically address the CBI, a large test vehicle based on 22-nm fully depleted silicon on insulator (FD-SOI) technology platform and WLP technology is described. In particular, CBI during drop test and temperature cycle on board is investigated and its failure mode analysis is discussed. The impact of silicon die thickness and ball grid array (BGA) metallurgy is also explored.

Key words: Wafer Level Packaging (WLP), Redistribution layer (RDL), Chip Board Interaction (CBI), Drop test, Temperature Cycle on Board (TCoB) test

INTRODUCTION

The continuous demand for miniaturization and higher functionality in electronic devices drive the adoption of small form-factor packaging architectures. Wafer Level Packaging (WLP) has been widely adapted by industry as one of best candidates to address this demand. On the other hand, 22-nm FD-SOI technology platform is an advanced silicon node for energy-efficient applications that delivers high (FinFET-like) performance. Combining both technology will make it more attractive for various markets such as 5G mmWave, Internet of Things (IoT), wearables, and automotive.

Unlike the flip chip (FC) architecture, WLP does not have mechanical support from a laminate structure, thus large die sizes become very sensitive to rigorous reliability tests. The application of underfill is often limited, which plays a critical role in moisture or mechanical shock mitigation. The lack of a laminate or sometimes even underfill raised significant challenges of how to control CBI, which can be traced to the thermomechanical deformation and stresses induced by the coefficient of thermal expansion (CTE) between the WLP and the printed circuit board (PCB).

Since 22-nm FD-SOI platform targets power-optimized high performance, the role of ultra-low dielectric constant (ULK) layers in silicon back end of line (BEOL) processing is critical. The use of the ULK layer to boost electric performance is well known but it may adversely affect structural integrity of devices due to its intrinsically lower mechanical strength and fragile nature[1].

To systematically address these chip board interaction (CBI) related challenges, a test chip with various CBI sensor macros was designed and fabricated based on 22-nm FD-SOI technology. To expand the current common industry WLP die size envelope, a large test chip of 7 x 7 mm^2 was designed. Based on the JEDEC standard, CBI reliability testing was carried out at board level and electrical read-outs were measured. To understand the roles of solder metallurgy and die thickness, different ball grid array (BGA) solder balls and die thicknesses were investigated during board level testing. Interestingly, the results show performance differences with different failure modes; in general, a thinner die performs better during both drop and temperature cycle (TC) testing. After drop testing, failures due to redistribution layer (RDL) cracks were a dominant failure mode, whereas TC testing failures were due to BGA soldier fatigue as a main failure mode.

TEST VEHICLE

To perform CBI analysis, a large CBI test vehicle (TV) was designed based on 22-nm FD-SOI technology. Figure 1 shows layout of the test vehicle. Test vehicle size was 7.0 mm x 7.0 mm. While most WLP products on the market stay with form factor of less than 6.0 mm x 6.0 mm due to reliability concerns at the board level, in this work larger die size was intentionally chosen to address potential issues beyond the current comfort zone.

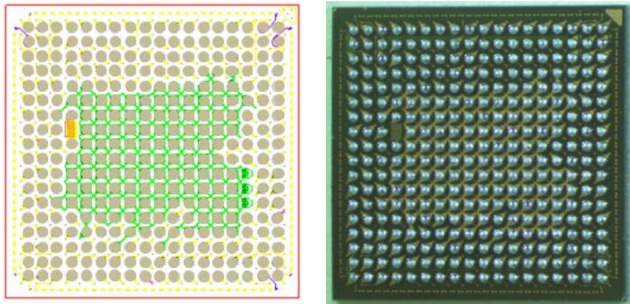


Figure 1. Layout (left) and optical image (right) of CBI test vehicle.

Within the test vehicle, several CBI sensors were integrated as shown in Table 1. Key area of focus of the study was die corners and peripheral area, where it experiences high Distance to Neutral Point (DNP), die center issues[2]. To address complete structural integrity from a silicon die level to board level, CBI sensors have been fully integrated in the BEOL processing. The WLP stich sensor in combination with a daisy chain between WLP package and PCB board was used to verify the overall integrity during board level reliability stress test.

Table 1. List of test sensors for reliability tests

Test sensors	***Purpose***
Perimeter Line Ring	Check mechanical integrity for die seal (Resistance / Leakage)
Perimeter Line Stitch	
Perimeter Line Top layer	
Delamination Sensor	Check mechanical integrity for die seal with better local resolution than perimeter line (Resistance)
WLP stitch	Stitch for test of adhesion between LB and RDL and ball integrity during board level reliability
Edge stitch	Assessment of interconnect die – RDL based on chains
THB Sensor	Sensitive humidity sensor in die edge (Leakage)
Serpentine via chain + comb	Assessment of damage in typical BEOL structures (Resistance / Leakage)

WAFER LEVEL PACKAGING PROCESSING

The wafer was continuously processed through WLP line for additional RDL construction. CBI sensors were re-routed through 1 layer of copper (Cu) RDL to solder balls. Key attributes are reported in Table 2. Since a large test vehicle was intentionally designed, the under-bump metallization (UBM) layer was adapted to improve CBI reliability performance. Additional RDL and UBM layers are captured in Figure 2.

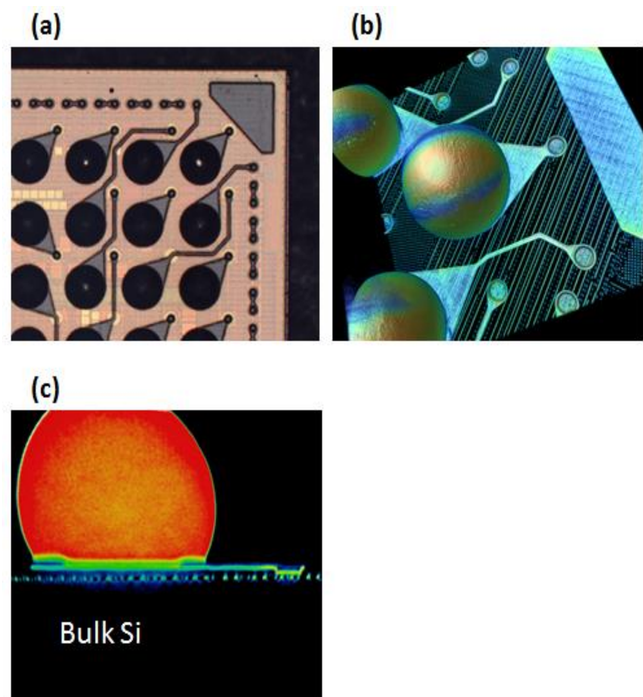


Figure 2. Key WLP features. (a) a die corner top-down optical image, (b) Slanted 3D X-ray, and (b) Cross-sectional X-ray over a BGA and RDL.

Table 2. WLP key attributes

Package Size (mm)	7 x 7
Number of RDL layer	1 Cu RDL
Polymeric Dielectric	polybenzoxozole (PBO)
RDL L/S (μm)	10 / 10
Number of I/Os	~ 300

DESCRIPTION OF CBI TESTING

The PCB board for board level reliability (BLR) testing was designed according to the JEDEC standard[3]. The PCB was

constructed of 8 layers with a dimension of 132 mm by 77 mm, as shown in Table 3.

Table 3. PCB test board stack-up

Board Layer	Thickness (microns)	Copper Coverage (%)	Material
Solder Mask	20		LPI
Layer 1	35	Pads + traces	Copper
Dielectric 1-2	65		RCC*
Layer 2	35	40% including daisy chain links	Copper
Dielectric 2-3	130		FR4†
Layer 3	18	70%	Copper
Dielectric 3-4	130		FR4†
Layer 4	18	70%	Copper
Dielectric 4-5	130		FR4†
Layer 5	18	70%	Copper
Dielectric 5-6	130		FR4†
Layer 6	18	70%	Copper
Dielectric 6-7	130		FR4†
Layer7	35	40%	Copper
Dielectric 7-8	65		RCC*
Layer 8	35	Pads + Traces + daisy chain links	Copper
Solder Mask	20		LPI

* Suggested RCC Material: Polyclad PCL-CF-400 12/35/35
† Suggested FR4 Material: NELCO N-4000-6 or equivalent

Figure 3 shows layout of a PCB test board, where total fifteen units can be surface mounted to the board in a 3 x 5 matrix. Surface mounted units established a daisy chain connection between the board and the units. Each unit has individual input and output traces, which routed to the end of the board for *In-Situ* resistance measurements.

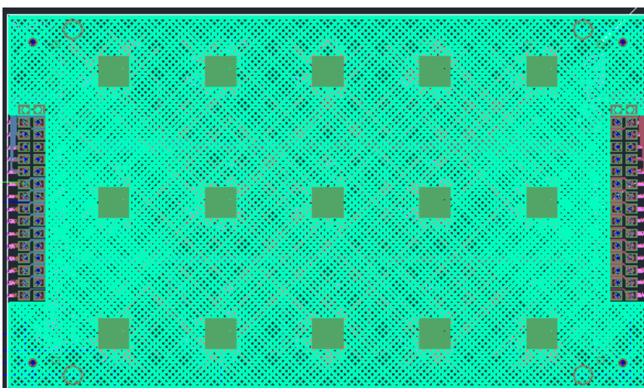


Figure 3. PCB test board layout.

DROP TEST

The drop tests were conducted as defined in JEDEC recommendations[3]. Once the TVs were surface mounted, the test PCB was mounted above the drop table via four screws in a horizontal way with the test units facing downward to apply the most significant board deflection. The test board traveled vertically through guided rails and collided with a strike surface at impact pulse of 1500 Gs within 0.5 ms (JEDEC condition B) repeatability applied, as shown in Figure 4. The board was connected to a data acquisition system with event logger, such that continuous resistance measurement of each unit was monitored in-Situ.

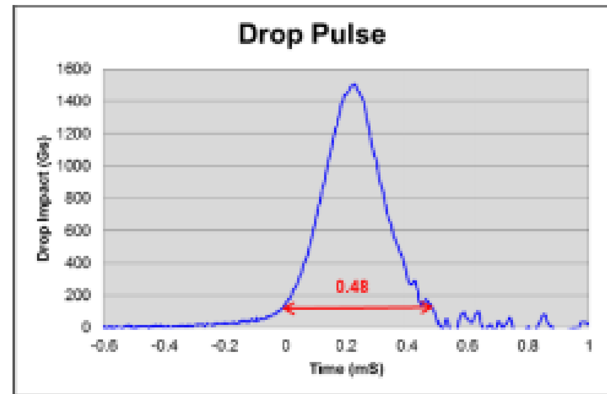


Figure 4. Input acceleration pulse during drop test.

In order to investigate CBI, three different groups were fabricated and tested as a cornering study. Each group consists of 15 units, as shown in Table 4. Two different silicon die thickness and different BGA metallurgies were selected as main variables. It is important to highlight that all drop tests were performed without any application of underfill and passed Drop 100x, without any failure. Figure 5 shows testing result in a Weibull plot. Since all three groups passed well beyond spec, testing was stopped at 1000x.

Table 4. Cornering study of three different groups and Weibull distribution analysis of drop test

	Group1	***Group 2***	***Group 3***
Si thickness (µm)	300	400	300
Alloy	SAC #1	SAC #1	SAC #2
Sample Size (EA)	15	15	15
First Time to Failure (FTTF) cycles	331	235	515
α (scale parameter)	1201	943	1411
β (shape parameter)	2.69	2.70	3.43

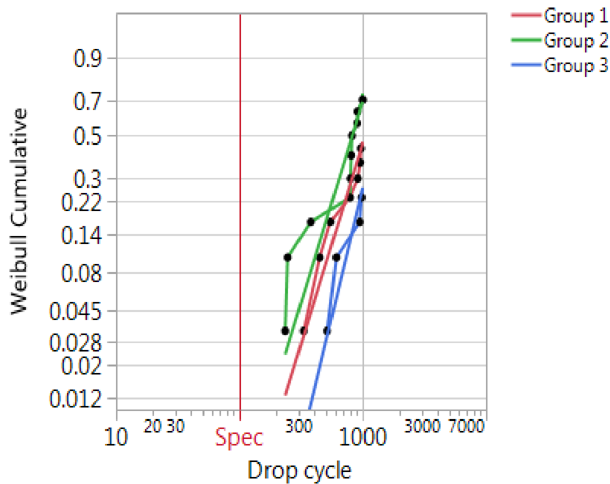


Figure 5. Weibull plot of drop test.

The effect of silicon die thickness

Comparison between Group 1 and Group 2 shows the effect of silicon die thickness. Silicon die thickness was controlled via wafer thinning process post RDL processing. Although there is limited data since the testing was stopped at 1000x, still the estimated result shows that die thinning by ~ 30 % provides improvement in both FTT and α (scale parameter or characteristic life). This result agrees with another study[4]. This phenomenon can be postulated such that thinner die has lower gravitational mass, in turn, this causes less inertia and momentum, and therefore less impact upon accelerated drop test.

The impact of BGA metallurgy

Group 1 and Group 3 were selected to investigate the effect of BGA, SnAgCu (SAC) metallurgy on reliability performance during the drop test. Test result in Table 4 and Figure 6 shows SAC #2 outperforms SAC #1 during board level drop test. Table 5 summarizes key material property of SAC. Compared to SAC #1, SAC #2 has slightly higher Young's modulus. But it is important to note that higher tensile strength of SAC #1, which allows it to withstand higher loads in tension and provides resistance upon failure during drop tests.

Table 5. Key material property of SAC

Property	*SAC #1*	*SAC #2*
Coefficient of Thermal expansion, CTE (ppm/ºC)	21	21
Tensile Strength (MPa)	49	91
Young's Modulus (GPa)	50.6	51.7

After completing the drop test, the PCB was underfilled, followed by a failure mode analysis on failed units. As indicated by the shape parameter (β > 1) in Table 4, the failure mechanism was based on wear-out. Figure 6 shows that major failure was RDL and polymeric dielectric layer cracking, initiated from interface between dielectric, UBM and BGA solder that continued to propagate through the RDL. In Group 2, resin layer cracking near the pad location was also observed. As expected, intermetallic compound (IMC) growth was very minimal and only occurred during the surface mount stage, so it did not contribute to any failures. This observation falls into common failure modes reported by another study[6].

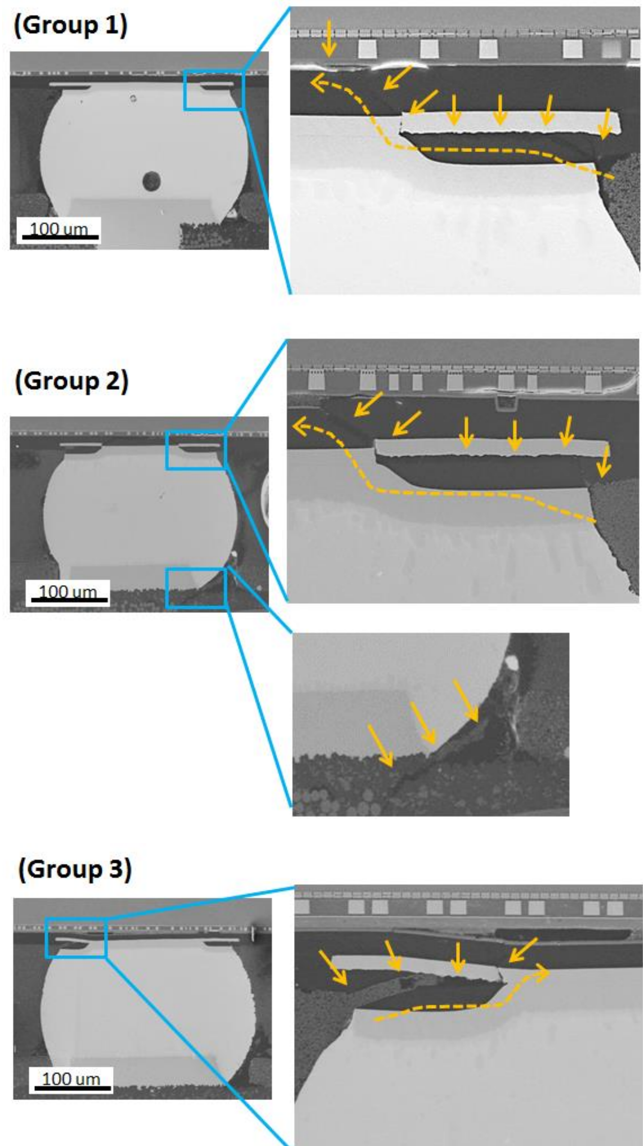


Figure 6. Cross-sectional images of drop test failures.

TEMPERATURE CYCLING TEST

As described in Table 6, some cornering study groups were subjected to temperature cycling test. According to JEDEC[5], -40/125ºC (condition G, shown in Figure 7) was used for temperature cycling on board (TCoB) testing. Similar to the drop tests, all testing was performed without application of

any underfill and its resistance measurement was tracked via *In-Situ* monitoring.

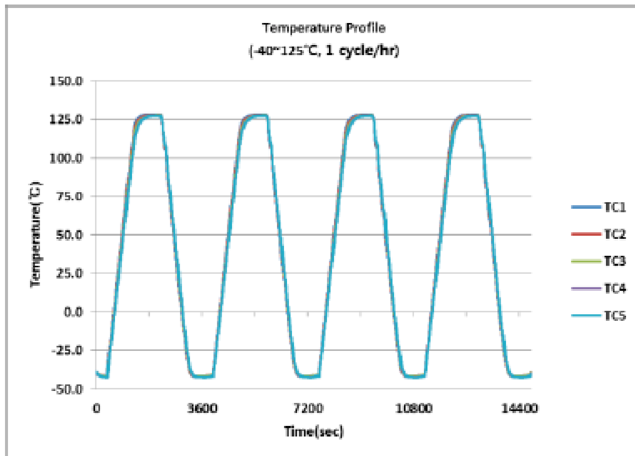


Figure 7. Temperature cycling profile.

Table 6. Cornering study of three different groups and Weibull distribution analysis of TCoB test

	Group1	*Group 2*	*Group 3*
Si die thickness (µm)	300	400	300
Alloy	SAC #1	SAC #1	SAC #2
Sample Size	15	15	15
FTTF cycles	418	493	659
α (scale parameter)	641	626	1164
β (shape parameter)	5.37	9.11	4.09

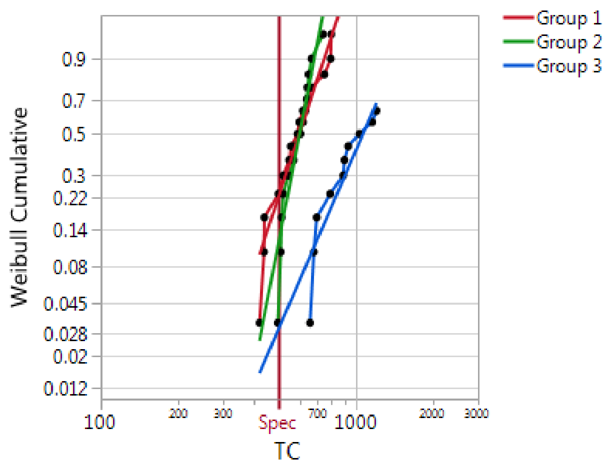


Figure 8. Weibull plot of TCoB

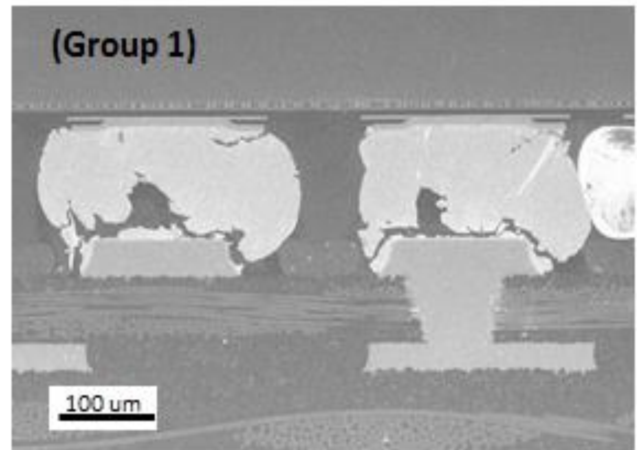
The effect of silicon die thickness

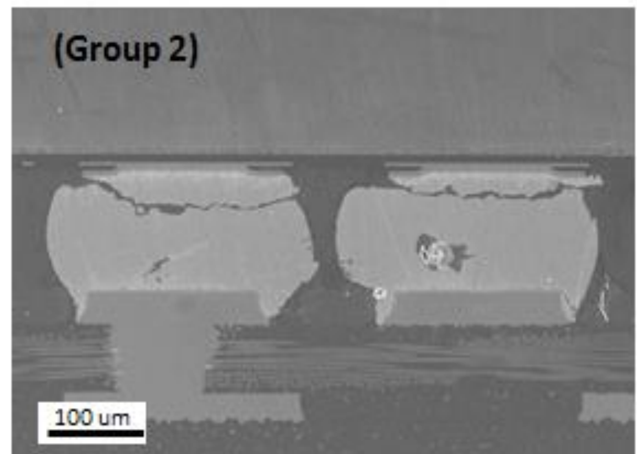
In contrast to drop test, the effect of silicon die thickness on TCoB is not obvious. Thinner die showed earlier first time failure but slower wear-out behavior. It appears it is comparable in this thickness range.

The impact of BGA metallurgy

Test result shows that SAC #2 exhibits consistently better performance than SAC #1, as shown in Table 6 and Figure 8. SAC #2 has same CTE as SAC #1 so there is no difference in CTE mismatch. Again, higher tensile strength seems to be the main driver for better reliability performance during TCoB tests. As expected, failures mainly occurred to the most outer corner BGAs, where higher stress/strain exists.

After completing TCoB testing, the PCB was underfilled and analyzed by cross sectioning the failing units. Failure mode analysis post TCoB also shows typical failure modes, as mentioned in Reference 5. Figure 9 shows representative cross-sectional images for each group.





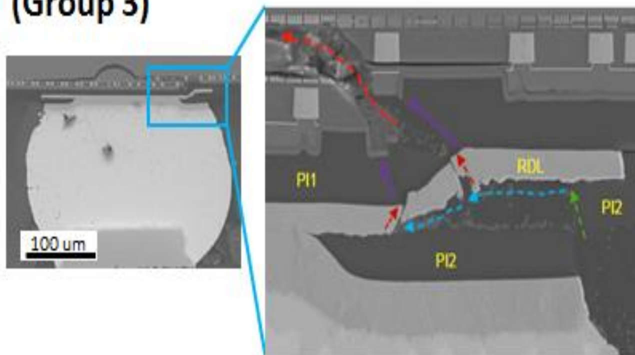


Figure 9. Cross-sectional images of TCoB failures.

CONCLUSION

This paper discussed the CBI investigation of a WLP-based 22-nm FD-SOI technology. To further expand current the CBI envelop, a large test vehicle was design and fabricated. Subsequently, the WLP test vehicle was subject to drop and TCoB tests. The TVs behavior was continuously monitored during board level reliability tests, to determine the impact of varying Si die thickness and solder ball metallurgy.

Post drop test failure analysis shows that RDL cracking is very common as a root cause for failure. A thinner die and higher tensile strength solder showed improved performance. In contrast, solder fatigue and RDL cracks were common for TCoB tests. Higher tensile strength solder showed better performance; however, the effect of silicon die thickness was not confirmed. All the Weibull analysis showed shape parameter greater than 1, which indicates the reliable maturity of 22-nm FD-SOI and WLP technologies.

22FDX is a registered trademark of GLOBALFOUNDRIES' 22-nm fully depleted silicon on insulator technology.

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