A New RDL-First PoP Fan-Out Wafer-Level Package Process with Chip-to-Wafer Bonding Technology

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***Abstract* — Fan-Out Wafer-Level Interposer Package-on-Package (PoP) design has many advantages for mobile applications such as low power consumption, short signal path, small form factor and heterogeneous integration for multi-functions. In addition, it can be applied in various package platforms, including PoP, System-in-Package (SiP) and Chip Scale Package (CSP). These advantages come from advanced interconnection technology called a redistribution layer (RDL).**

However, a PoP-type RDL-base platform requires dual-side RDLs on both top and bottom sides to stack another package on top. In a monolithic process flow, that means the second RDL only can be fabricated after finishing all the first RDL and the assembly processes such as flip-chip bonding, molding and grinding. Therefore, this process flow is not quite as advantageous as a non-PoP type platform because chips can be lost during the second RDL process.

In this paper, to address this RDL-base Interposer PoP challenge, a real chip-last process flow with a chip-to-wafer (C2W) bonding technology is introduced. And the results are presented of building and testing an RDL-base wafer-level Interposer PoP with a size of 12.5 x 12.5 mm^2 and thickness of 0.357 mm including solder ball. The bottom side has a 3-layer RDL structure and the top RDL for the package stacking has a 1-layer structure. These RDLs are implemented with copper (Cu) lines with 5 µm/10 µm of line & space (L/S) and copper (Cu) cored solder balls (CCSBs) are used as the vertical interconnect components. The silicon die and CCSBs' joint quality is confirmed by reliability testing. The test vehicle package passed all the reliability tests of moisture resistance test (MRT) L3, Temperature Cycle, Condition B (TCB) 1,000 cycles and high temperature storage (HTS) 1,000 hrs.

Keywords—Fan-Out package, FOWLP, Chip-to-wafer, C2W, Interposer PoP, Chip-last, RDL-first, PoP

I. INTRODUCTION

Interposer Package-on-Package (PoP) is an enabling packaging technology to satisfy the requirements of a three-dimension (3D) structure by stacking two different laminate substrates (top interposer and bottom substrate) with copper (Cu) cored solder balls (CCSBs) or through mold vias (TMVs) for vertical interconnections. Using two substrates provides the benefits of easier warpage management and flexible construction with lower cost. The package warpage can be controlled by optimizing the substrate materials and design. The top interposer contributes design flexibility for either commercially available or customized memory use. For these reasons, Interposer PoP is mostly used for mobile application processors (APs)

Although Interposer PoP based on laminate substrate technology is a very powerful platform to satisfy the current demands in the industry, it still has limitations in reducing package thickness and body size due to a limited capability in current substrate manufacturing. In addition to the package size limitations, advanced packages for the 5G era require higher input/output (I/O) quantity which needs finer interconnections, fine bump pitch and multiple chips.

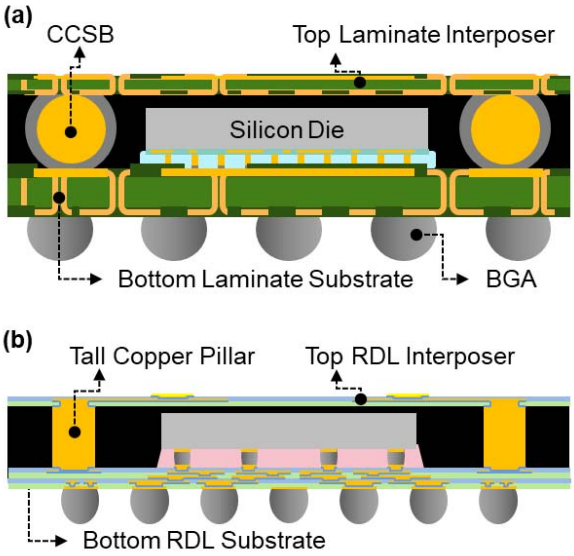

Figure 1. Illustration of Interposer PoP: a) Laminate-based; b) RDL-based.

Many companies are focusing on new material and assembly technology to satisfy the new requirements mentioned above. One of the promising technologies in the market is a Interposer PoP platform utilizing Cu redistribution layer (RDL) technology which is already applied in flagship mobile processors. This RDL-based 3D package has many advantages such as form factor, feature size, electrical and thermal benefits [1, 2]. Figure 1 shows two different Interposer PoPs: (a) laminated-based, and (b) RDL-based.

RDL manufacturing technology is based on wafer processing which enables thinner and finer electrical traces. RDL is conventionally fabricated by an additive layer method on a silicon (Si) or glass wafer. By repeated build-

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up of a passivation layer and a metal interconnection layer, multiple RDLs are possible. Each metal line is mechanically and electrically connected through vias patterned in the passivation layers.

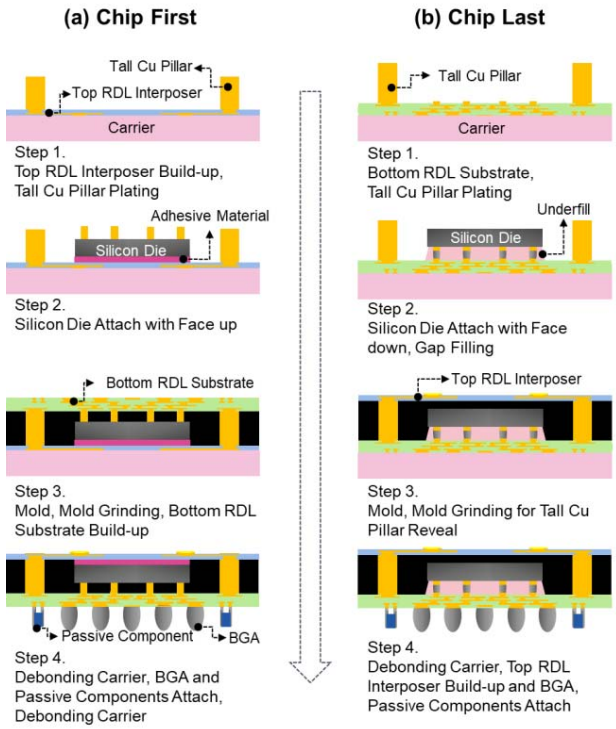

Figure 2. Illustration of Process Flow: a) Chip First; b) Chip Last.

There are two major process concepts for the RDL-base Interposer PoP as shown in Figure 2: (a) chip first, and (b) chip last. In the chip-first process, chips are bonded face-up on a with or without interposer RDL layer and then encapsulated with an epoxy molding compound (EMC) material. For electrical connections, metal pads on the chip are exposed by wafer grinding. Finally, multiple RDLs are fabricated on the mold exposed side. This multiple RDLs acts as the bottom RDL substrate. The chips are attached on the wafer before the fabrication of the complex multiple bottom RDL layers. The chip-last process has an opposite process flow to the chip first. The bottom RDL substrate layer is first prepared on a wafer and then the chips are flip chip bonded as shown in Figure 2 (b). The top RDL interposer can be fabricated in demand.

The two options have their own merits and demerits regarding yield management and build cycle-time control. However, if both top and bottom RDL layers are required, both options cannot avoid a risk of chip loss, because at least one (top or bottom) RDL layer should be fabricated after the chip bonding. This process flow also impacts the process cycle-time increment, because of the sequential process flow.

A new hybrid assembly process has been introduced that can overcome the technical barriers mentioned above. A sample build was conducted with a fan-out type test vehicle to assess package characteristics regarding structure and reliability. A key difference of the new process is that each RDL is prepared separately and assembled after the chip attachment. One of the benefits of this process is that interim tests prior to the actual chip assembly step can identify known-good sites. The actual chips can then be allocated only on the known-good RDL sites. In other words, the actual chip loss during the RDL process can be prevented by separating the RDL preparation. Another benefit is a sample handling efficiency because both top and bottom RDL layers are formed directly on carrier wafers without any intermediate materials such as EMC underfill. Therefore, the wafers provide a flat surface during the RDL process and, eventually, those process features contribute overall yield improvement of the RDL and assembly process.

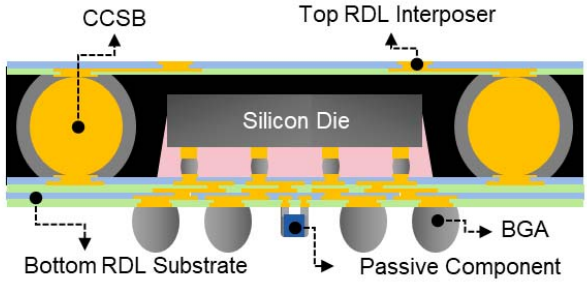

Figure 3. Illustration of RDL-based Interposer PoP with CCSBs

Instead of tall copper pillars for the vertical interconnection, CCSBs are applied in the hybrid process like the laminate-base Interposer PoPs shown in Figure 3. The latest RDL-based 3D packaging platform adopts tall copper pillar. However, in this new process, the electroplated copper pillars may not provide robustness during the assembly process. CCSB technology is a well-known and mature approach for the vertical interconnections in laminate-based mobile packages because it can control the gap height between the top interposer and bottom substrate due to un-melting the Cu core balls during the mass reflow process [3-6].

This work provides the results of a test vehicle build using the new process flow and its reliability performance. The advantages will also be discussed in following sections.

II. TEST VEHICLE INFORMATION

A. Package Structure

Figure 4 shows a 3D illustration of the Interposer PoP test vehicle. It is composed of a silicon die, CCSBs, top RDL Interposer RDL layer and bottom RDL layer. The silicon die is flip bonded on the bottom RDL substrate with 45 µm bumps for the peripheral array and 65 µm bumps for the core array pitched micro-bumps. An EMC material is filled between these two RDL layers and encapsulates the die and the CCSBs.

The top RDL interposer layer has array of under-bump metal (UBM) pads for electrical connections with mobile

memory packages or passive components such as capacitors and inductors. The signal path of the top RDL interposer is expanded to the bottom RDL layer through the CCSBs connecting vertically between the two layers. The pitch of the 360 CCSBs is 250 µm.

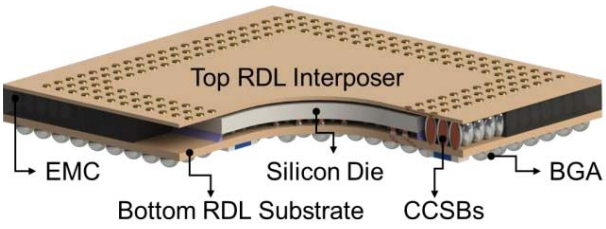

Figure 4. 3D illustration of the RDL-based Interposer PoP.

The bottom RDL substrate consists of three metal layers and four dielectric organic passivation layers. The minimum line and space (L/S) width of the bottom RDLs is 5 µm and 10 µm, respectively. This fine width of the metal interconnection lines improves the signal integration while maintaining a limited package size. The encapsulating EMC provides structural robustness, electrical insulation and environmental protection for the silicon die and CCSBs. A ball grid array (BGA) is formed under package bottom side. The solder ball height after soldering by mass reflow and the pitch are 135 µm and 350 µm, respectively. The top RDL interposer and bottom RDL substrate are the same size of 12.5 x 12.5 mm^2. Total package thickness including the solder ball is 357 µm. Table 1 summarizes the information of the test vehicle package.

TABLE I. THE INFORMATION OF THE TEST VEHICLE

	Silicon Die	**Top RDL Interposer**	**Bottom RDL Substrate**
Size [mm^2]	8.7 x 9.1	12.5 x 12.5	12.5 x 12.5
Thickness [µm]	100	22	45
I/O diameter [µm]	Peripheral: 45 Core: 65	240	215
I/O pitch [µm]	90	350	350
I/O count [ea]	2800	560	880

B. Daisy Chain Design

The test vehicle has daisy chains for electrical open/short (O/S) testing before and after the reliability tests. A total of seven daisy chains are embedded that can be divided into three major interconnection paths as shown in Figure 5: (a) bottom RDL to top RDL, (b) bottom RDL to silicon die and (c) bottom inter-RDL path.

The bottom RDL to top RDL path checks the vertical connectivity with three daisy chains. One of these three chains loops around the four package corners which are the most susceptible areas to the thermal cycling test. The other two chains are for the package core area and the top RDL interposer area. The bottom RDL to silicon die path is designed to test the micro-bump joints between the bottom RDL substrate and the silicon die. The last path checks the metal interconnection lines inside the bottom RDL substrate. These daisy chains help identify failed locations before and after the reliability tests.

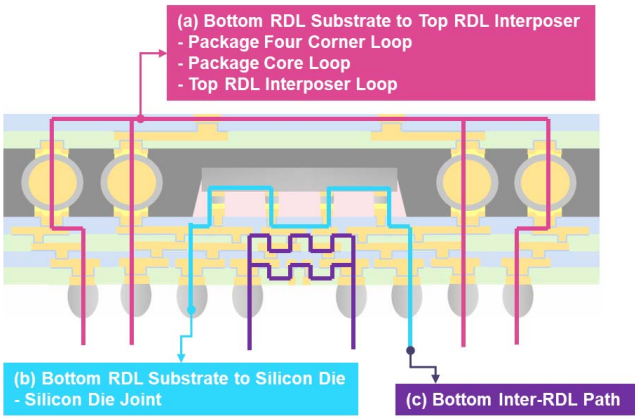

Figure 5. Schematic figure of the three daisy chains' paths.

III. PROCESS FLOW

A. Preparation of Top and Bottom RDL

As mentioned, the separate build-up of the top and bottom RDL layers before die attachment is the key advantage of this new process. Each RDL is prepared at the wafer level. Figure 6 illustrates preparation sequences. The wafer act as a temporary carrier which will be removed in the final fabrication stage.

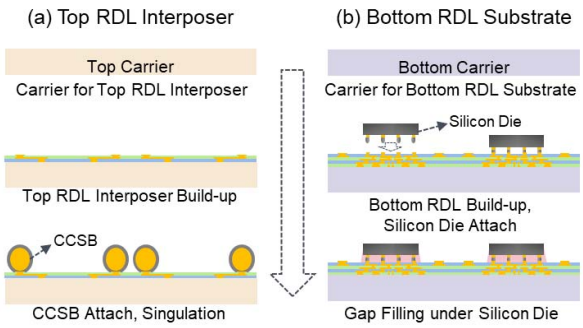

Figure 6. Preparation of (a) top RDL interposer and (b) bottom RDL substrate.

The top RDL interposer consists of single layer of Cu metal lines and UBM pads for the CCSBs. An organic passivation material encapsulates the metal interconnections. The CCSB is dropped on each UBM Pad and reflowed in the wafer level as shown in Figure 6-a. Each top RDL interposer is singulated for flip chip attachment on the bottom RDL substrate wafer.

The bottom RDL substrate has multiple layers of metal lines. The same organic material is applied between the lines. The silicon chips are flip chip bonded on the bottom RDL wafer. By inspecting the bottom RDL before the die attach, the silicon chips can be attached only on known-good sites. That avoids losing expensive application-specific integrated circuit (ASIC) chips in actual production. A conventional mass reflow process can be applied for the flip chip bonding because the bottom RDL wafer has little warpage unlike thin organic substrates. The gap between the die and bottom substrate is filled with an underfill material as shown in Figure 6-b.

B. *Assembly of Top Interposer and Bottom RDL Substrate*

After separate preparation, the singulated top RDL interposers are flip bonded onto the bottom RDL substrate wafer as shown in Figure 7. All the samples can be inspected to eliminate any flaws before bonding, so known-good top interposers are attached only on known-good bottom substrate sites. This is one of the key advantages of separating the two RDLs.

In the next step, gap filling between the top and bottom layer is accomplished using a molding process at the wafer level. The molding compound completely fills the gap without any voids. Then, the wafer piece on each single top RDL layer is removed by laser irradiation process. A temporary carrier is bonded to the top RDL layer for substrate carrier debonding and BGA attachment processes. After mounting the BGA on the bottom RDL substrate by a mass reflow process, singulation was performed to the final single packages.

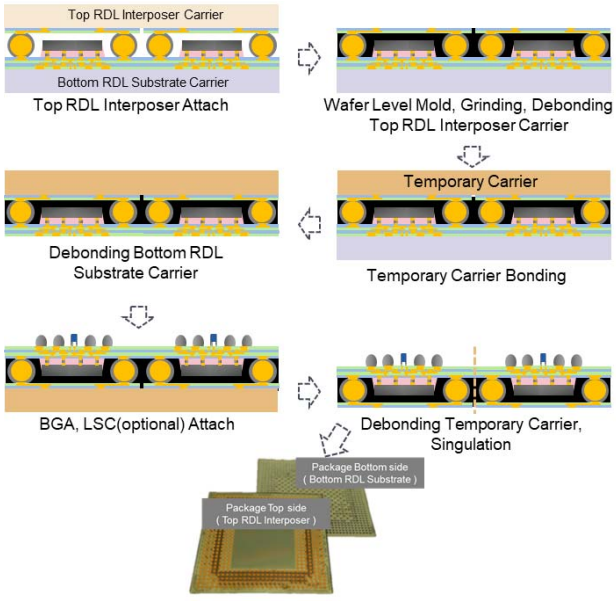

Figure 7. Process flow for RDL-based Interposer PoP with CCSBs.

IV. KEY TECHNOLOGIES AND FABRICATION RESULT

The RDL-base Integrated PoP is manufactured with three key technologies: (a) wafer support system (WSS), (b) RDL fabrication and (c) CCSBs for the vertical interconnections.

A. *Wafer Support System (WSS)*

Thin top and bottom RDLs are prepared simultaneously utilizing WSS technology. The temporary carrier wafer acts as a support structure during the RDL fabrication because the thickness of the RDL layers is less than 50 µm. Most available WSS processes utilize a sacrificial layer applied between the carrier wafer and the RLD for easy separation. The sacrificial layer material can be a liquid or a film type. It should stand high temperature processes without any degradation or delamination. There are several separation methods such as thermal sliding, chemical etching, mechanical detachment and laser irradiation. The carrier wafer also needs to maintain its flatness through all the RDL processing. Therefore. all the material properties and characteristic should be carefully reviewed and tested for stable fabrication.

B. *RDL Technology*

The introduction of RDL technology has led to visible changes in Interposer PoP that impact form factor and L/S for the electric signal path. To fabricate the bottom RDL substrate, four layers of dielectric organic passivation and three layers of copper metal lines are sequentially built-up. Finally, landing UBM pads are plated for the silicon die and CCSB attachment. The minimum L/S is 5 µm/10 µm and total thickness is 45 µm with UBM. Figure 8 shows representative cross-sectional images of the bottom RDL substrate.

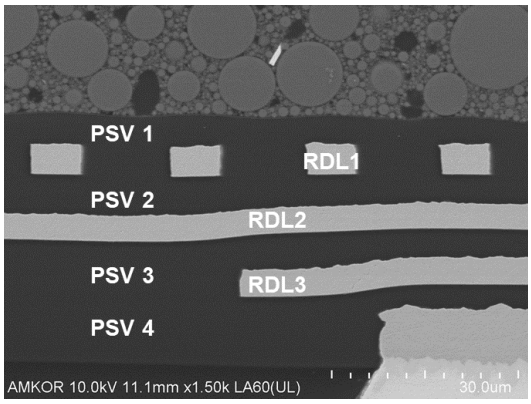

Figure 8. Cross-sectional images of the bottom RDL substrate.

One of the major benefits of using RDLs for the Integrated PoP is the thickness reduction. The package thickness of the RDL-based Integrated PoP is about 30% thinner than a conventional laminate-based package. Figure 9 illustrate the thickness comparison between a laminate and an RDL Integrated PoP.

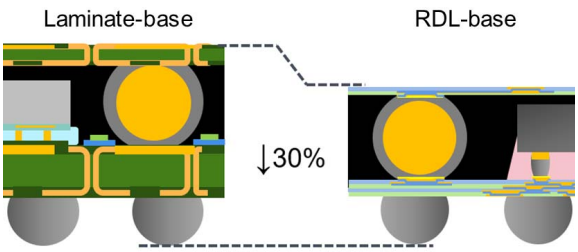

Figure 9. Comparison between a laminated and an RDL-based Interposer PoP

C. CCSB as a Vertical Interconnection

CCSB is one of the representative components for vertical interconnection between the top and bottom RDL substrates. The CCSB is composed of three materials: the Cu core ball, a nickel (Ni) layer and solder cladding. The size of CCSB should be chosen by both package height and CCSB landing pad pitch/diameter to avoid any solder bridge or non-wet problem during the CCSB drop process or the top interposer bonding process. Figure 10 shows cross-sectional images of the RDL-based Integrated PoP test vehicle.

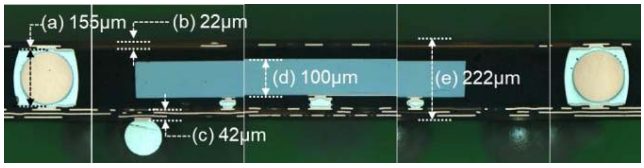

Figure 10. Cross-sectional image: a) CCSB b) Top RDL Interposer c) Bottom RDL Interposer d) Silicon Die and e) Pkg. thickness except BGA

V. RELIABILITY PERFORMANCE

Component level reliability (CLR) testing was performed on the RDL-based Integrated PoP test vehicles. Testing was performed in accordance with the JEDEC standard as shown in Table I. The test d samples passed all the requirements: (a) Thermal cycle (TC) condition B of 1,000 cycles after Moisture Sensitivity Test (Precon) L3/260°C condition, (b) High temperature storage (HTS) of 1,000 hrs without Precon. Table I shows reliability test items, conditions, sample quantities and results.

All samples were checked by electrical O/S testing and scanning acoustic tomography (SAT) testing (see Figure 11). Figure 12 and 13 show the cross-sectional images of micro-bump joints and CCSBs after TC 'B' and HTS test. The joints showed no abnormality after all the reliability tests.

TABLE II. RELIABILITY TEST CONDITIONS AND RESULTS

Reliability test items	Condition	Read points	Sample #	Results
Precon (L3)	L3 / 260°C	-	76	Pass
TC 'B'	-55°C / 125'C	1000x	76	Pass
HTS	150'C	1000hrs	73	Pass

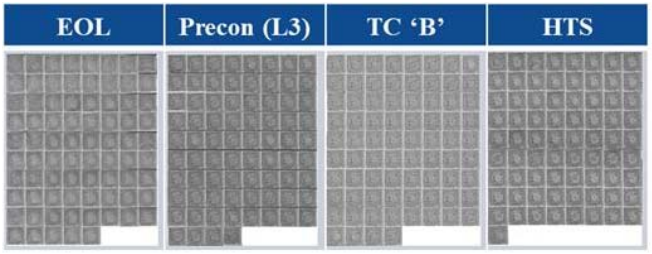

Figure 11. SAT images.

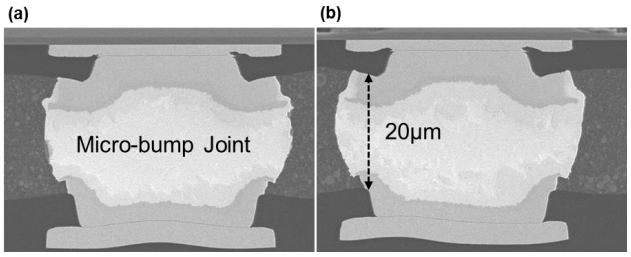

Figure 12. Cross-sectional images of Silicon die mirco-bump joint: a) TC 'B' 1000 cycles with Precon L3 and b) after HTS 1000 hrs.

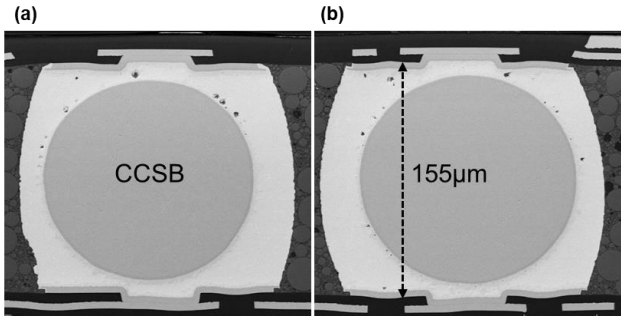

Figure 13. Cross-sectional images of CCSB joint: a) TC 'B' 1000 cycles with Precon L3 and b) after HTS 1000 hrs.

VI. CONCLUSIONS

A new RDL-based Integrated PoP process has been developed and evaluated by reliability testing. The separate build-up of the top and bottom RDL leads to cost reduction because the silicon chip loss can be minimized by attaching to only known-good sites. It also shortens the assembly cycle-time because the two the RDLs are fabricated in parallel. In comparison to a build-up process from one side RDL to the other side RDL sequentially, the benefits are as follows:

- Increasing capability for yield management: mapping known-good sites by an interim test enables a selective assembly minimizing any loss of good chips.
- Shortening cycle-time: separate fabrication of both top and bottom RDLs in parallel.
- Decreasing form factor: the RDL-based Integrated PoP is ~30% thinner than current mass-produced laminate-based Integrated PoP.

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