# Challenges and Approaches to Developing Automotive Grade 1/0 FCBGA Package Capability

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***Abstract*— Automotive Grade 1 and 0 package requirements, defined by Automotive Electronics Council (AEC) Document AEC-100, require more severe temperature cycling and high temperature storage conditions to meet harsh automotive field requirements, such as a maximum 150°C device operating temperature, 15-year reliability and zero-defect quality level. Moreover, increased integration of device functionality to meet the new automotive requirements for in-vehicle networking, autonomous driving, infotainment and sensor integration are driving increases in die and package sizes. This paper provides an update on flip chip ball grid array (FCBGA) package development as quality and reliability requirements increase for larger and larger package form factors and approaches that should be taken to meet Grade 1/0 requirements. Package quality and wear-out failure modes and mechanisms experienced during extended reliability testing in Automotive Grade 2 and 3 package qualifications have identified thermomechanical stress and material degradation at high temperatures as key factors for focus in Grade 1/0 development. To achieve higher grade levels, key package substrate materials such as core, solder resist and build-up layers need to be evaluated as well as assembly materials such as underfills materials may need improvement.**

**Mechanical simulation data of key material properties such as coefficient of thermal expansion (CTE), modulus of elasticity (E1) and glass transition temperature (Tg) of the substrate and assembly materials are used to provide guidance for the selection of substrate and assembly materials used in the design of experiments to meet Auto Grade 1 and 0 reliability requirements.**

**Taguchi mechanical simulations results show that use of low CTE materials for the substrate core and build up material was beneficial in preventing SR cracking, UF cracking and bump cracking. Reliability stress results on design of experiments based on inputs from simulation resulted in developing a substrate and assembly material set that meets AEC100 solder resist (SR) Grade 1 and 0 package requirements on a 45-mm x 45-mm FCBGA.**

***Keywords-FCBGA, Auto-grade, AEC, FEM, Taguchi***

## I. INTRODUCTION

Increased digital processing content in automobiles, ranging from infotainment applications to Advanced Driver Assist System (ADAS), is necessitating a thorough evaluation of the reliability performance of flip chip ball grid array (FCBGA) semiconductor packages. Depending on the function, the component level reliability requirements are classified by the Automotive Electronics Council (AEC) as Grade 3, Grade 2, Grade 1 or Grade 0. The requirements for these grade levels are summarized in TABLE I. The requirements for Temperature Humidity Bias (THB), biased and unbiased Highly Accelerated Stress Test (HAST) remain the same across all automotive grades – 96 hours at 130$^0$C /85% humidity or 264 hours at 110℃ /85% humidity. All reliability testing is followed by electrical testing at room and hot temperature.

TABLE I. AUTOMOTIVE GRADE-LEVEL REQUIREMENTS [1]

| Stress | Condition | Duration | | | |
|---|---|---|---|---|---|
| | | Grade 0 | Grade 1 | Grade 2 | Grade 3 |
| Temperature-Humidity-Bias (THB) | 85$^0$C/85%RH | 1000 h | 1000 h | 1000 h | 1000 h |
| Biased Highly Accelerated Stress Test (HAST) | 110$^0$C/85%RH | 264 h | 264 h | 264 h | 264 h |
| Unbiased Highly Accelerated Stress Test (uHAST) | 110$^0$C/85%RH | 264 h | 264 h | 264 h | 264 h |
| | 130$^0$C /85%RH | 96 h | 96 h | 96 h | 96 h |
| Temperature Cycling (TC) | C: -65$^0$C-150 $^0$C | | 500x | | |
| | H: -55$^0$C-150$^0$C | 2000x | 1000x | | |
| | B: -55 $^0$C-125$^0$C | | | 1000x | 500x |

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| | | | | | |
|---|---|---|---|---|---|
| High Temperature Storage Life (HTSL) | 175$^0$C | 1000x | 500x | | |
| | 150$^0$C | 2000x | 1000x | 1000x | 1000x |
| | 125$^0$C | | | 1000x | 1000x |
| Power Temp Cycle (PTC) (Required for Parts rated at >1W) | -40$^0$C-150$^0$C | 1000x | | | |
| | -40$^0$C-125$^0$C | | 1000x | | |
| | -40$^0$C-105$^0$C | | | 1000x | 1000x |

It becomes apparent that the stringent temperature cycling and high temperature storage requirements for Auto G1/0 drive the need for careful selection of both substrate and assembly materials. Larger temperature ranges of -65$^0$C to 150$^0$C exacerbate many of the failure mechanisms associated with temperature cycling, such as fatigue cracking of solder bumps as well as cracking of polymeric materials such as underfills and solder resist (SR) films. Similarly, the high temperature storage test conditions (HTSL: 150$^0$C and 175$^0$C) result in permanent changes in the material properties that can result in performance degradation of packages. The long cycle times for reliability data collection also means failures in qualification could result in substantial product qualification delays. Hence, judicious use of thermomechanical modeling is needed through-out the development and qualification process.

The common material degradation mechanisms encountered in FCBGA packages at different reliability stresses are summarized in TABLE II.

TABLE II. MATERIAL DEGRADATION MECHANISMS

| | TCx | HTS |
|---|---|---|
| Solder | Bump cracking | Solder consumption, IMC growth |
| Underfill | Cracking | Oxidation, cracking |
| TIM[1] | X | Delamination |
| Substrate | PTH cracking, micro-via cracking, SR cracking (leading to trace cracking) | |

1 thermal interface material

Polymeric materials undergo permanent changes when subjected to high temperatures for extended periods of time. Depending on the ambience, this may include material oxidation as well as mechanical property changes resulting in embrittlement. The presence of humidity can also lead to loss of adhesion at the die passivation and substrate solder mask interfaces. Lin et al have studied the evolution of tensile properties and creep behavior of underfills under isothermal aging at various temperatures and developed a 4-parameter empirical model to predict the property changes [2]. The monotonic increase in modulus and tensile strength of the underfills with isothermal aging at temperatures above and below the Tg of the underfill was reported along with an increase in elongation to break suggesting an overall toughening of the underfill material.

Likewise, solder joints in the FCBGA packages undergo thermal aging resulting in growth of relatively brittle intermetallic layers, adversely impacting the mechanical behavior of solder joints [4].

In addition, there is a strong interaction between design rules and materials. Often, the best materials available in the market cannot meet the reliability requirements of Auto-G1/0 without restrictive design rules for substrates and assembly. The design rules, while enabling the demonstration of higher reliability, may adversely impact the electrical performance and/or result in higher cost. As a result, there is a continuous effort to re-enable restrictive design rules over time through materials and process improvements.

Lastly, due to the mission critical functions of the automotive components, there is emphasis on defect elimination and containment as well. This is best achieved by stringent quality control measures which include failure mode effects analyses (FMEAs), materials and process control plans across the entire packaging supply chain. Thus, there are three components to achieving Automotive Grade 1/0 certification – materials selection, substrate and assembly design rules and robust manufacturing systems (see Figure 1. ). The paper focuses on materials selection via thermomechanical simulations and assembly experiments and reliability testing.

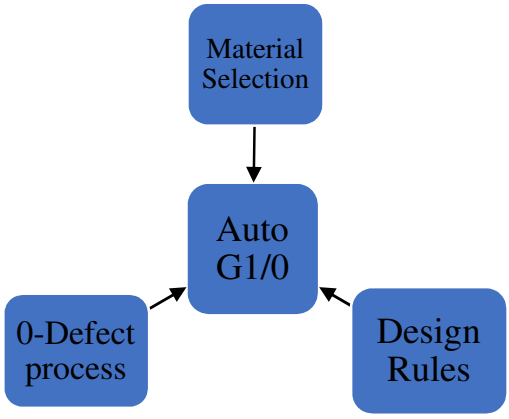


Figure 1. Components of Automotive Grade1/0.

## II. MECHANICAL SIMULATION STUDIES

The impact of material properties of the package substrate and assembly materials on solder resist cracking, underfill cracking and chip interconnect cracking was studied using the Taguchi method of analysis. The main material properties investigated were coefficient of thermal expansions (CTE1, CTE2), elastic modulus (E1) and glass transition temperature (Tg) of the substrate core material, build up material and solder resist material as well as the underfill material in assembly. Three levels (low, medium, high) of each material property were simulated using commercially available materials. For example, three core materials with CTEs of 4, 7.6 and 15 ppm/C were compared. TABLE III. shows the material properties investigated.

TABLE III. PROPERTIES OF SUBSTRATE AND ASSEMBLY MATERIALS

| Factor / Level | Core | | BU | | SR | | | | UF | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] |
| 1 | 4 | 20 | 10 | 4 | 9 | 50 | 4 | 100 | 20 | 80 | 3.8 | 100 |
| 2 | 7.6 | 24 | 23.8 | 8.5 | 20 | 98 | 8.4 | 125 | 35 | 100 | 8 | 125 |
| 3 | 15 | 40 | 40 | 25 | 60 | 150 | 17 | 150 | 52 | 135 | 11 | 150 |

The Taguchi simulation method was used to determine the impact of the material properties for each of the three failure mechanisms: solder resist cracking, underfill (UF) cracking

and chip interconnect bump cracking. Figure 2. shows the impact of varying material properties on the propensity for solder resist cracking at the die corner solder bumps. The Taguchi output is a signal to noise ratio (S/N) with 0 being equivalent to no stress. Higher numbers (absolute value) indicate higher stress. Figure 2. shows that SR and UF material have a large influence on SR cracking. Low modulus of the SR and low CTE of the UF results in improving resistance to SR stresses.

| Factor / Level | Core | | BU | | SR | | | | UF | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] |
| 1 | 4 | 20 | 10 | 4 | 9 | 50 | 4 | 100 | 20 | 80 | 3.8 | 100 |
| 2 | 7.6 | 24 | 23.8 | 8.5 | 20 | 98 | 8.4 | 125 | 35 | 100 | 8 | 125 |
| 3 | 15 | 40 | 40 | 25 | 60 | 150 | 17 | 150 | 52 | 135 | 11 | 150 |

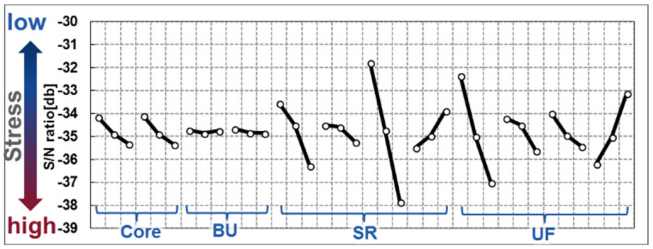


Figure 2. Impact of material properties on SR cracking.

Figure 3. shows the impact of varying material properties on the propensity for UF cracking at the die corners. The core material and UF material have a large influence on UF cracking. Low CTE core materials and underfills with low CTE, low modulus and high Tg lower the propensity for UF cracking.

| Factor / Level | Core | | BU | | SR | | | | UF | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] |
| 1 | 4 | 20 | 10 | 4 | 9 | 50 | 4 | 100 | 20 | 80 | 3.8 | 100 |
| 2 | 7.6 | 24 | 23.8 | 8.5 | 20 | 98 | 8.4 | 125 | 35 | 100 | 8 | 125 |
| 3 | 15 | 40 | 40 | 25 | 60 | 150 | 17 | 150 | 52 | 135 | 11 | 150 |

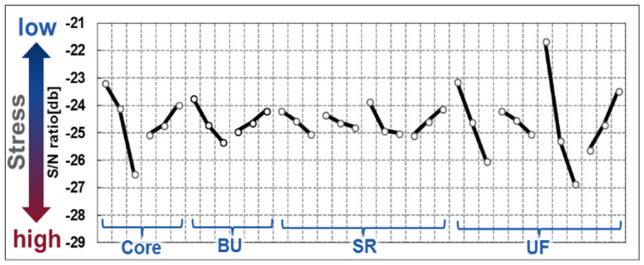


Figure 3. Impact of material properties on UF cracking.

Figure 4. shows the impact of varying material properties on the propensity for chip interconnect bump cracking. The substrate core and buildup materials and UF material have a large influence on bump cracking. Low CTE core material, low modulus buildup material and underfills with high modulus can be used to lower bump cracking risks.

| Factor / Level | Core | | BU | | SR | | | | UF | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | E1 [GPa] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] | α1 [ppm/°C] | α2 [ppm/°C] | E1 [GPa] | Tg [°C] |
| 1 | 4 | 20 | 10 | 4 | 9 | 50 | 4 | 100 | 20 | 80 | 3.8 | 100 |
| 2 | 7.6 | 24 | 23.8 | 8.5 | 20 | 98 | 8.4 | 125 | 35 | 100 | 8 | 125 |
| 3 | 15 | 40 | 40 | 25 | 60 | 150 | 17 | 150 | 52 | 135 | 11 | 150 |

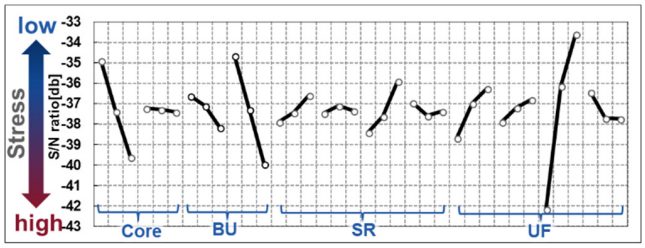


Figure 4. Impact of material properties on chip-interconnect bump cracking.

From the results shown in Figure 2, 3 and 4, it becomes apparent that optimizing substrate and assembly material properties to reduce risk of one mechanism may adversely increase risk of another failure mechanism, resulting in necessary tradeoffs. Figure 5. shows a composite for all three fail mechanisms. In general, material properties need to be optimized for the dominant failure mechanism observed for a specific package geometry while at the same time also modified to prevent another failure mechanism from becoming dominant. Based on material property trends shown in Figure 4, general recommendations would be to use a low CTE core material with low modulus buildup material and with a solder resist that has low CTE and modulus. For underfills, while a low CTE and high Tg are beneficial, modulus has a strong influence. A low modulus UF is recommended for UF and SR crack prevention but significantly increases bump cracking risk for which a high modulus UF is desired.

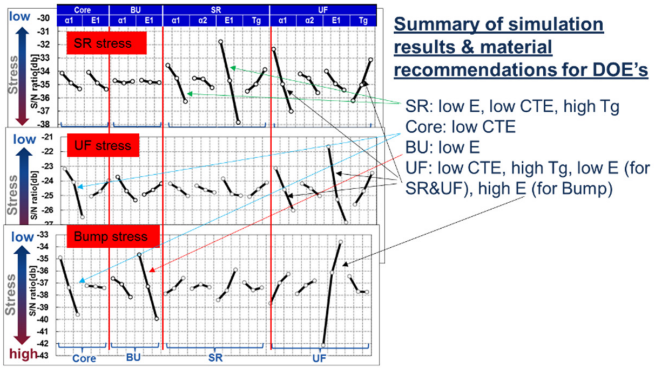


Figure 5. Comparison of impact of material properties on all three mechanisms (SR cracking, UF cracking and bump cracking).

Results and recommendations from the Taguchi simulations were used as a guide in selection of current and new materials for design of experiments (DOEs) to meet AEC 100 Grade 0 and 1 reliability requirements.

## III. SUBSTRATE AND ASSEMBLY MATERIALS DOE'S

A daisy chain test vehicle (TV) was used for assessing different commercially available substrate and assembly materials. The TV die was 19.2 mm x 19.2 mm with copper phosphate (CuP) bumps at 165-um pitch. The TV die was flip chip attached to a 45-mm x 45-mm, 2-2-2 organic substrate with a 0.8-mm core and a 1-mm thick copper heat spreader attached to the package substrate. SAC 305 solder was used on both CuP bumps and BGAs. A schematic of the package crross-section is shown in Figure 6.

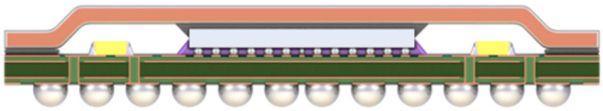

Figure 6. Cross-section schematic of the 45-mm FCBGA package used in this study.

The DOE consisted of evaluating substrates with two core materials (core 1, core 2), two buildup (BU) materials (BU1, BU2) and two solder resist materials (SR1, SR2). Three substrate types were fabricated using a combination of core, buildup and SR materials as shown in TABLE IV. The material properties of the substrate materials are shown in TABLE V.

TABLE IV. SUBSTRATE MATERIALS USED FOR THE THREE TYPES OF SUBSTRATES FABRICATED.

| Substrate Type | Core | Build up | Solder Resist |
|---|---|---|---|
| Substrate type 1 | Core 2 | BU 2 | SR 1 |
| Substrate type 2 | Core 1 | BU 1 | SR 1 |
| Substrate type 3 | Core 1 | BU 1 | SR 2 |

TABLE V. MATERIAL PROPERTIES OF SUBSTRATE MATERIALS USED IN THE DOES

| Substrate Material | CTE 1 (ppm/C) | CTE2 (ppm/C) | Modulus (E1) (GPa) | Tg (C) |
|---|---|---|---|---|
| Core 1 | 6 | 3 | 23 | 260 |
| Core 2 | 9 | 4 | 23 | 260 |
| BU 1 | 23 | 78 | 8 | 154 |
| BU 2 | 46 | 120 | 7 | 156 |
| SR 1 | 38 | 115 | 5 | 130 |
| SR 2 | 33 | 90 | 4 | 175 |

FCBGA assembly was performed using four different underfill materials (UF1, UF2, UF3 and UF4). The other assembly materials such as thermal interface material (TIM) and copper lid attach material were kept the same for all builds on the three types of substrates. The physical properties of the four UF materials evaluated are shown in TABLE VI. .

TABLE VI. PHYSICAL PROPERTIES OF THE FOUR UNDERFILLS EVALUATED

| Underfill Material | CTE 1 (ppm/C) | CTE 2 (ppm/C) | Modulus (E1) (GPa) | Tg (C) |
|---|---|---|---|---|
| UF1 | 28 | 105 | 10 | 90 |
| UF2 | 28 | 89 | 10 | 130 |
| UF3 | 22 | 89 | 9 | 154 |
| UF4 | 29 | 96 | 8 | 156 |

DOE samples assembled were subjected to reliability testing after Level 3 preconditioning was performed. Reliability stress tests done were a) Unbiased HAST (uHAST) (110°C/85% RH) for 264hrs, b) temperature cycle condition H (-55°C to 150°C) for 1000 and 2000 cycles and c) High temperature storage (175°C) for 500 and 1000 hours. Open/short (OS) tests were done on some legs. Approximately 10 samples/leg were removed after preconditioning and after each of the reliability readouts and visually inspected for fillet cracking after lid removal. Scanning acoustic tomography (SAT) analysis was done to identify any underfill delamination and units were cross-sectioned and planar polished to inspect for solder resist cracking, bump cracking, and underfill cracking at each readout.

## IV. DOE RESULTS

One leg with substrate type 1 (low CTE core, low CTE buildup) and with UF1 passed O/S testing after all reliability testing to AEC-100 grade 0 (264 hrs uHAST, 2000 cycles TCH, 1000-hrs HTS at 175°C). Optical, SAT, X-section and planar polishing did not reveal any evidence of damage such as solder resist cracking, fillet cracking or bump cracking after 264 hrs UHAST, 2000 cycles TCH and 500 hrs HTS at 175°C. Representative images of the inspections are shown in Figure 7. However, small UF fillet surface cracks were seen on units after 1000 hrs HTS at 175°C. Cross-section analysis showed that the fillet surface cracks were contained within a thin discolored region of the underfill fillet. The discolored region is believed to be a thin skin of oxidation-damaged underfill epoxy. Some of the underfills did not exhibit this surface fillet cracks.

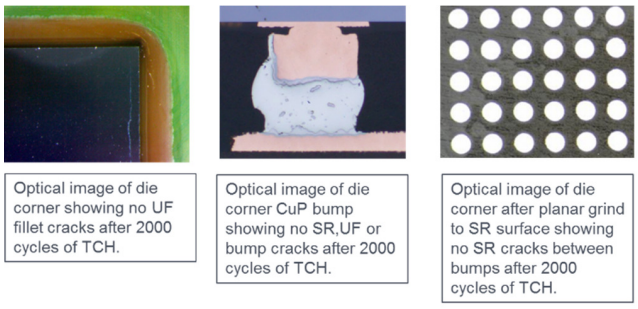


Figure 7. Optical images of units after 2000 cycles TCH showing no evidence of SR, UF or bump cracking.

## V. DISCUSSION AND CONCLUSIONS

Both Taguchi mechanical simulations results and DOE reliability results show that use of low CTE materials for the substrate core and build up material was beneficial in

preventing SR cracking, UF cracking and bump cracking. For underfill properties, mechanical simulation results indicate that a compromise needs to be made between the use of a high modulus material for bump crack resistance and a low modulus material needed for solder resist and underfill cracking resistance. The DOE results showed that underfill (UF1) with an intermediate modulus performed the best and met Grade 1 and 0 reliability requirements. The anticipated benefits of using a high Tg UF material could not be realized in the DOE results.

A new phenomenon of underfill fillet surface cracks seen only after 1000 hrs of HTS at 175°C for some underfills is believed to be related to underfill epoxy and/or hardener degradation by high temperature oxidation. While these surface cracks do not result in electrical failures, further investigation is necessary to understand the kinetics of the oxidation and to partner with underfill material suppliers to formulate underfills with more resistance to oxidation. Alternate underfills did not exhibit this surface oxidation.

In conclusion, Taguchi mechanical simulation results were predictive in determining the impact of substrate and assembly material properties on the propensity for solder resist cracking, underfill cracking and bump cracking. Reliability stress results on design of experiments based on inputs from simulation resulted in developing a substrate and assembly material set that meet AEC100 Grade 1 and 0 package requirements on a 45-mm x 45-mm FCBGA package.



## REFERENCES

[1] AEC - Q100 Rev - H: Failure Mechanism Based Stress Test Qualification For Integrated Circuits (base document).

[2] C. Lin, J. C. Suhling, P. Lall, , "Isothermal aging induced evolution of the material behavior of underfill encapsulants," 59th Electronic Components and Technology Conference, 2009.

[3] Z. Lin, V. Subramanian, P. Malatkar, N. Ananthakrishnan, "Understanding Underfill Degradation in Reliability Testing Conditions for ADAS Package Development," 68th Electronic Components and Technology Conference, 2018.

[4] V.L. Nguyen, C-S. Chung, H-K. Kim, "Mechanical Behavior of Sn-3.0Ag-0.5Cu/Cu Solder Joints After Isothermal Aging," Journal of Electronic Materials, vol.45, No.1, 2016, pp 125-135.