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THE GLOBAL DEMAND FOR DATA increases day-by-day. Whether it is security cameras like Ring, smart speakers from Amazon or Google, or streaming devices and services such as Roku and Apple Plus, as the number of smart devices around us grows, the data they communicate grows exponentially. By some estimates, there are 10 billion Internet of Things (IoT) devices (see Figure 1), transmitting 30 exabytes (EB) (30*10^{18} bytes) of data/month. 70% of that data is in the form of streaming video today. The video content of this data is expected to grow to 80% by 2022. At the same time, the data transmission rate will increase to exceed 1 Terabits per second (Tbps) near the middle of this decade[1].

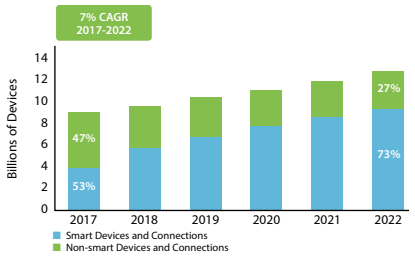

Figure 1. IoT devices will grow from 10 billion today to 12 billion by 2022.
Source: Cisco VNI Mobile, 2019.

This extensive data transmission puts a tremendous burden on hyperscale data centers that carry most of the information. As customers reach out for these services, data centers need to react quickly to ensure the information is returned to customers in a timely fashion, without any delay. This means the networking devices at the data center need to handle a large amount of data at faster speeds.

Virtualization and software defined networking (SDN) have resulted in multiple layers of switching within the hyperscale data center. Data may travel between a top of rack (TOR), leaf and spine switch in the data center before it is sent back to the consumer. In older data centers, North-South traffic with TORs connected together was common. In contrast, the Hyperscale data centers employ SDN and virtualization with more East–West traffic. The data is split between many servers, which creates the need for leaf and spine switches.

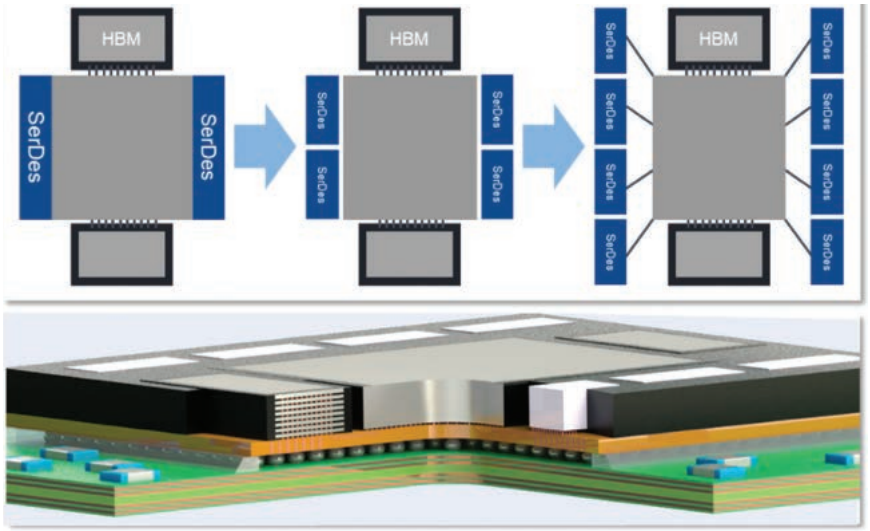

Figure 2. An example of discrete I/O and IP reuse.

Integrated Packaging Solutions

To improve the performance of high-performance switches, there is a growing trend to bring the different building blocks closer to each other. Traditionally, all these building blocks would be integrated on a system on chip (SoC) but there are two problems with that approach. One, is that such an SoC can become too large – even larger than the reticle size. In advanced process nodes, like 7 nm, the cost of such a device may be too high. The other problem is that as die get larger, the yields fall off quickly. This makes an already expensive solution even more expensive.

To address this situation and provide a third alternative, engineers are increasingly looking into the chiplet approach with multiple smaller dies integrated in a single package. Only the logic portion that needs to be at a smaller process node stays at that node, other analog or serializer/deserializer (SerDes) functions, or memory are designed and processed on a larger process node die. The different dies still stay close to each other within the same package. The chiplet approach helps reduce the overall cost, improve the individual yields and deliver good performance. Some customers are also looking into splitting the logic die into two parts resulting in "die-partitioning." This improves the yield for the large logic die even further.

Figure 2 shows an example of how some system designers' architect their solutions. An application-specific integrated circuit (ASIC) with a SerDes and high

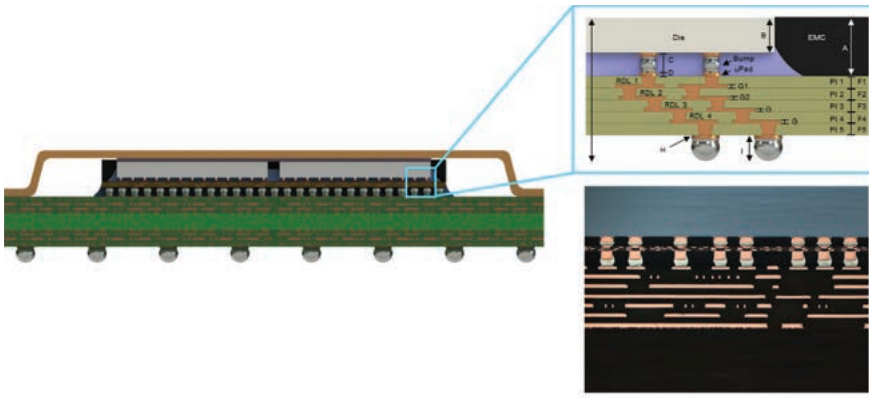

Figure 3. S-SWIFT® packaging employs multi-layer copper and organic dielectric RDLs.

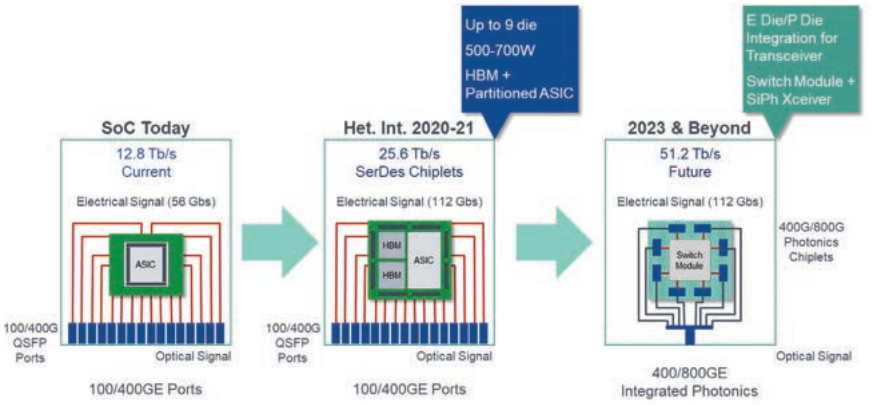

Figure 4. The progression of the switch roadmap will lead to integrated silicon photonics solutions.

bandwidth memory (HBM) provides the complete solution. The number of HBMs in these designs has been increasing with some solutions looking into as many as 6-8 HBM stacks in one package. Discrete I/O chips are used because SerDes I/O chips do not scale well with process nodes and may be able to stay in an older, less expensive silicon node. This allows the reuse of intellectual property (IP) as this same die can be used in other products and increases the total number of I/O's beyond what is possible in a single SOC die.

There are many ways to address package-level integration of different types of semiconductor technologies or Heterogeneous Integration. One is the multi-chip module (MCM) approach with different die attached to the package substrate. A second approach uses high-density modules, examples are 2.5D construction, which uses a silicon interposer to connect the different dies together. Another approach uses high-density fan-out (HDFO) technology, to fabricate the interposer in Cu and organic dielectrics. This eliminates the need for an expensive interposer die. The HDFO subsystem then can be placed on the package substrate. Amkor calls this type of structure S-SWIFT® (Substrate Silicon Wafer Integration Fanout Technology) packaging.

With added functionalities, the ASIC die seem to be approaching full reticle size. Integrated with discrete HBMs and SerDes chips, some package substrates are approaching 75 x 75 mm and 85 x 85 mm sizes today, with high density modules approaching 40 x 50 mm. Looking to the future, some of the packages will include silicon photonics and will get as large as 100 mm on each side.

For data rates above 50 Gbps, pulse-amplitude modulation with four levels (PAM4) is used to lower the Nyquist frequency and reduce the channel loss. To avoid the decreased signal to noise ratio (SNR), increased power and cross-talk issues that are associated with PAM, "a highly integrated system that can bring devices closer to each other in order to reduce the interconnect distance" is the long-term solution according to SEMI's Heterogeneous Integration Roadmap, 2019 Edition[2].

Advanced Multi-layer Packaging

SWIFT packaging is a High-Density Fan-Out (HDFO) technology developed by Amkor in 2013. This design technique allows multiple dies to be assembled together with RDL techniques in increasingly smaller and tighter geometries. It is a die-last process and therefore die are committed only to known good sites after fully fabricating the fan-out layers and using exhaustive AOI techniques determine good sites available for die attach. This helps to improve yields. With smaller geometries, SWIFT design provides better performance at a lower cost. It is already widely used for mobile applications and can also be used for Networking and High-Performance Computing (HPC) applications. Primary drivers for this advanced packaging design approach include:

- Reduced form factor
- Enhanced signal integrity
- Superior impedance matching
- Optimized power distribution

Figure 3 shows the typical construction of a substrate SWIFT or S-SWIFT (HDFO on substrate) structure. Typically, S-SWIFT design has a 4 RDL (RDL-first, chip last) construction Layer 1 and Layer 3 are used for signal routing and Layer 2 is used for the ground plane. Layer 4 can be used for mixed purposes – either as a plane or for copper pillar (CuP) interconnect.

S-SWIFT packaging can support bump pitches of 30 to 80 μm (typical), with line/spacing of 2/2 μm for RLD layers 1-4. Several customers are considering the use of SWIFT technology for integrating ASIC and chiplets (SerDes, HBM, and others). With its excellent electrical properties and flexibility, SWIFT technology is also a good candidate for die partitioned modules. Figure 3 shows how the multiple layers can be interconnected.

Looking at the roadmap of Networking devices, it seems heterogeneous packaging technology can be used in many different forms (see Figure 4). Today's Networking switch is a monolithic SoC in

either a 14 nm or 7 nm process node and typically supports 12.8 terabits per second (Tbps) capacity. Looking forward, several companies are looking into moving to a smaller process node and supporting 25.6 Tbps capacity. This is the architecture where Heterogeneous Integration starts making a difference. As chip sizes grows larger, there is a big push for separating ASIC logic functions from the I/O. To improve the system memory bandwidth, HBMs are also increasingly integrated with the ASIC within the same package. SWIFT packaging can be used to integrate ASIC, SerDes and HBM together. Amkor believes in not so distant future silicon photonics will also be part of this solution.

In the short-term, customers want to cost-optimize the high-performance computing solutions with the tools available to them. The high cost of wafers at 5 nm and 3 nm nodes will require partitioning large ASIC die into two parts, and, in some cases, accompanied by HBM in an HDFO or RDL module. SerDes I/O drivers, which do not need to be in a smaller geometry process as the rest of the logic, will be in the form of chiplets. The whole solution being implemented in a flip chip ball grid array (FCBGA) package with materials that have low dissipation factor (Df) and low dielectric constant (Dk) properties for very high speed signaling.

Silicon Photonics technology is making quick inroads into Switch market. Silicon Photonics building blocks can accept light signals and can convert them into electrical signals and visa-versa for data processing. Some of the challenges are that there is no common architecture for this solution. Different customers have steered towards different ways to integrate these technologies. Heterogeneous integration, optical alignment and assembly in high volume are still some of the big hurdles for the industry.

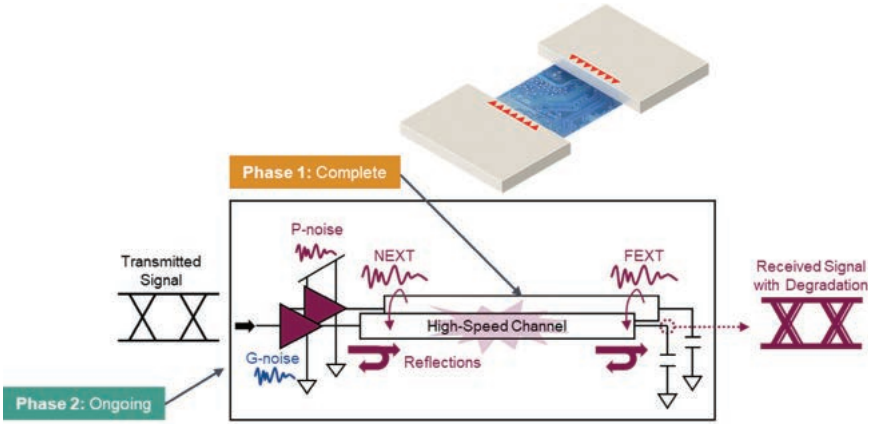

Figure 5. Power Distribution Network (PDN) transmissions and signal integrity are key aspects of advanced packaging.

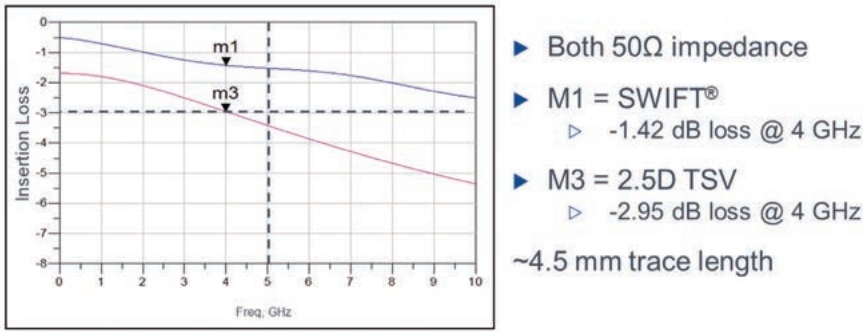

Figure 6. From the Phase 1 testing, the S-SWIFT® package provides much lower insertion loss than 2.5D TSV for signals routed from die to die – especially at high frequencies.

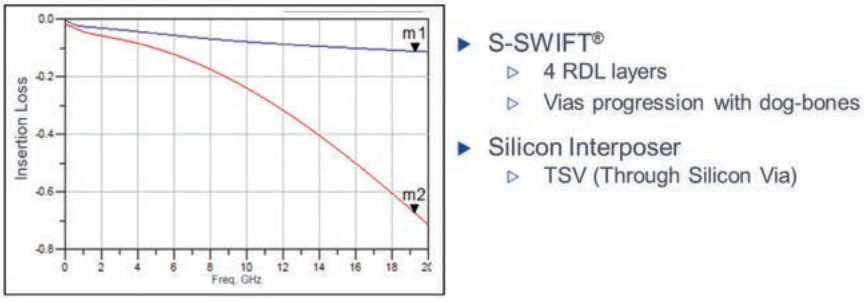

Figure 7. S-SWIFT® packaging provides much lower losses than a 2.5D TSV – Off Package.

The Technology Toolbox for Advanced Packages

To address some of the bottlenecks associated with large heterogeneous solution whether for Networking or High-Performance Computing (HPC) application, Amkor has developed a toolkit. Amkor's toolbox includes:

1. Large package sizes up to 85 mm on each side
2. Multiple die assembly and test capabilities
3. Advanced thermal interface materials (TIMs)
4. S-SWIFT packaging for high performance

Electrical Simulation

With SerDes supporting 112 Gbps rates and several die communicating with each other in the package, it becomes critical to run electrical simulations with accurate package models. These simulations should consider electrical paths as well as Power Distribution Networks. Amkor has capability to accurately model the signal path and has also modeled the expected power supply noise to give its customers a better understanding of the effect of package on the system perfor-

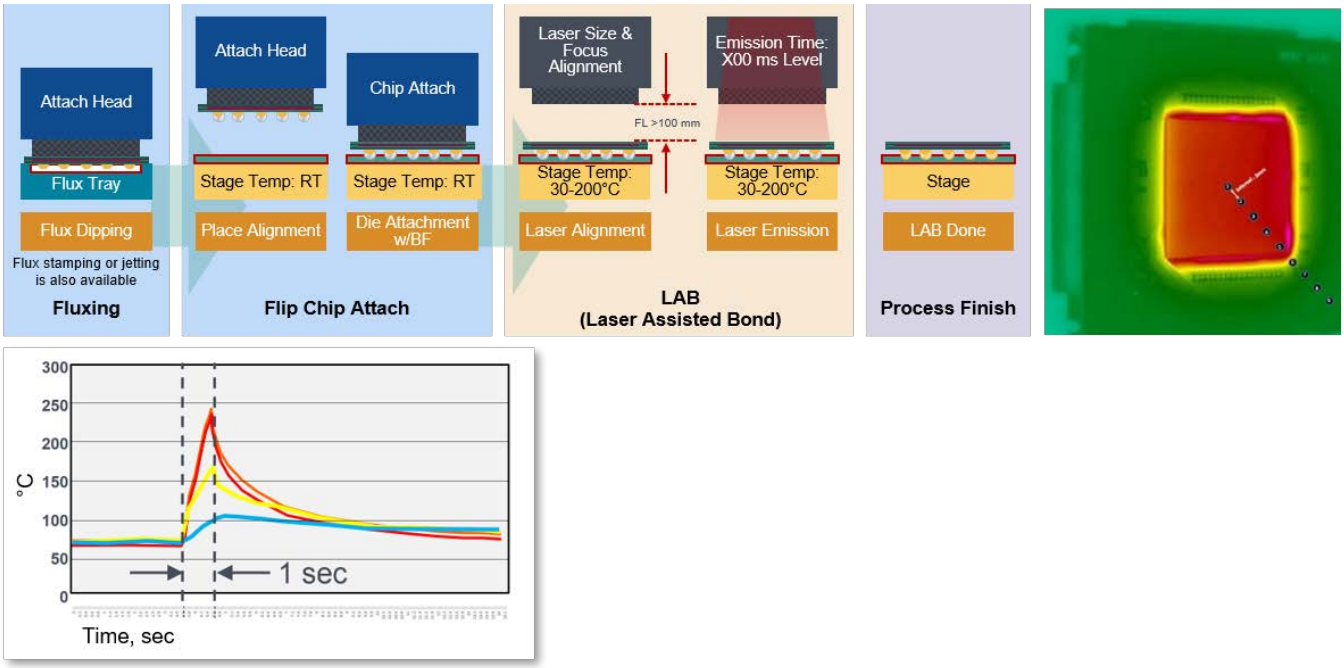

Figure 8. Laser-assisted bonding profiles in different areas in an HDFO package.

mance. Figure 5 shows a setup used by Amkor for simulation purposes. Simulations include both the signal path as well as ground and power supply noise.

As shown in Figure 6, S-SWIFT packaging shows much lower insertion loss compared to 2.5D signal routing in the interposer. Off-chip signals Through Silicon Via (TSV) packaging. With 2.5D structure, customers can expect 3 dB signal loss at around 4 GHz. The SWIFT structure can go beyond 10 GHz before hitting the 3 dB insertion loss mark. This shows the extra margin designers of an application can expect with SWIFT construction.

As shown in Figure 7, a SWIFT structure has lower losses compared to a TSV structure. These are signals going off-package.

With more functionality at higher speeds, an effective solution has a to deal with a large amount of power dissipation. It is not unheard of to have access of 500W of power that needs to be dissipated. Customers need to determine if they want their solution to be lidded or if they want to have a bare die with a stiffener ring. The TIM material that sits between the silicon and lid material or between lid and heat sink can plays a critical role in getting the heat out of the package. To determine the right choice, there are several developments underway to optimize thickness of the lid and TIM material selection, including commercialization of a lower-cost Indium metallurgical TIM.

Another challenge with large body heterogeneous packages is warpage. Warpage is unavoidable, but there are ways to limit it, to make the package yields better. One technology has helped in this area is Laser-assisted bonding (LAB). LAB Technology uses a laser to heat up the die locally and solders it to the substrate. Some of the advantages of LAB are:

- Avoids bulk heating and minimizes the coefficient of thermal expansion (CTE) mismatch between the IC and the substrate
- Provides excellent warpage control for large, thin substrates
- Means less side wall solder wicking

Figure 8 shows different aspects of using LAB technology. With local heating the die, bump and low-k layer stress levels can be lowered as the substrate expansion and contraction is minimized.

As part of our advanced packaging research, and especially for high speed networks, Amkor is working continuously to increase the number of chiplets in its designs and also increase the size of the S-SWIFT package. With HBMs moving from HBM2 to HBM2E and soon to HBM3, Amkor's close work with its customers will help us to be an integral part of this transition. Other efforts include plans to use embedded bypassing caps in new products at the module level. We are also looking into S-Connect technology to provide L/S of 1/1 for very high-density interconnects.

At Amkor, heterogeneous integration forms the basis of our most advanced packaging designs. To help customers meet the increasing performance demands of today's network systems; a variety of technologies are already offered. Ongoing development will provide even greater performance for signal transmission, power dissipation and long-term reliability while addressing the need for cost-effective packaging solutions for future networks. ◆

REFERENCES

[1] Cisco Visual Networking Index (VNI) Global and Americas/EMEAR Mobile Data Traffic Forecast, 2017-2022

[2] Heterogeneous Integration Roadmap, 2019 Edition, Chapter 2: High Performance Computing and Data Centers, IEEE.

Amkor helps customers deliver high performance network systems

Networking infrastructure is more critical today than ever before. Amkor offers packaging solutions with the high-power density, low-power consumption and reduced size to satisfy the latest design requirements.

As a stable, long-term OSAT, Amkor partners with networking customers to enable IC technologies by delivering processors, controllers, power management devices and memory and sensors products.

We provide technology expertise, intelligent package design, quality systems and highly capable manufacturing to meet the needs of networking customers.

Enabling the Future

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