Enhancing Punch MLF® Packaging with Edge Protection™ Technology

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Quad Flat No-Lead (QFN) semiconductor packaging provides a small form factor as well as good electrical and thermal performance for low cost. Add demonstrated long term reliability to its benefits and it is easy to see why it has been a preferred automotive package for many years. QFNs are offered in saw and punch formats with punch being a well-defined and used solution in the automotive market [2].

In spite of its wide usage, a long-standing concern with the punch form factor of *Micro*LeadFrame® (MLF®)/QFN packaging has been the tendency of the exposed corners and top edge flange areas to experience cracking after assembly during handling, electrical test operations, shipping and surface mount technology (SMT) printed circuit board (PCB) assembly. These gaps or micro-cracks may compromise the integrity of the package resulting in the semiconductor device's functionality and/or performance being compromised.

To resolve the issue of package cracks/gaps, Amkor Technology has developed a solution known as Edge Protection™ technology (EPT) [1]. EPT improves the robustness of the package by extending the molding compound encapsulate to the exposed edge areas of the top flange and corners. This white paper will provide background on MLF/QFN packaging identifying the concern and provide the details of the EPT solution that has demonstrated significant improvements while maintaining conformance with the Package Outline Drawing (POD).

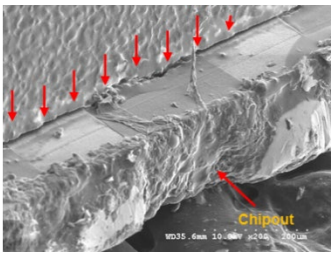
QLF PACKAGE BACKGROUND

In contrast to sawn QFNs that are used in many applications, the punch format of the *Micro*LeadFrame® MLF leadless packaging portfolio has long been an accepted and preferred solution for automotive applications. Large body (≥5 mm x 5 mm) devices with a dimple enabled wettable flanks have been utilized in non-automotive applications since the late 1990's and in automotive applications since 2008. In automotive applications, the need for robust packaging solutions is critical for long-term reliability considerations.

The incident of package corner and flange edge cracks and gaps has been a low parts per million (PPM) recurring event. In all instances, the crack/gap is considered a reliability concern since the integrity of the package has been compromised. Attempts to resolve the problem have resulted in significant improvements and reduced occurrences. However, in the case of automotive applications, elimination of the problem is a requirement. A reduction of incidents is not adequate.

Historically, resolution of the crack/gap issue has involved multiple improvements to the punch MLF manufacturing process, including singulation tooling design enhancements, material improvements, leadframe design modifications and tray design modifications. While these improvements made a positive impact, they did not completely resolve the incidents of crack/gap. These improvements were primarily focused on the assembly manufacturing process and did not address the additional handling processes and procedures occurring after assembly.

In the area of device electrical testing, there are multiple opportunities for the crack/gap phenomena to be introduced, resulting in same damage as seen during the assembly process. Items such as burn-in socket design and insertions, test contactor design and insertions, tray/tube designs introduced in the test handling operations or surface mount technology (SMT) processing, all have the potential to introduce the crack/gap previously thought to be associated only with the assembly manufacturing process. Incidents of package crack/gap have been caused by these non-assembly handling processes and procedures, with the damaged unit not being identified until after mounting on an end customer's printed circuit board (PCB) (see Figure 1).



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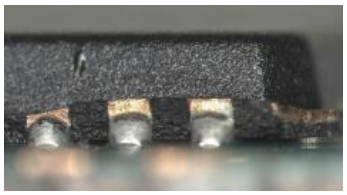

b.

Figure 1 | Punch Quad Flat No-Lead (QFN) devices with package crack/gap damage.

(a) SEM photo of edge crack – *note chip out damage caused by automated test equipment ATE handler insertion*
(b) Side view depicting cracked device that was discovered after mounting to PCB

IMPROVED MLF® PACKAGING

To resolve the assembly and non-assembly related failure mechanisms, a resilient package level enhancement for the punch MLF has been developed and implemented by Amkor Technology. Known as Edge Protection technology, this innovation addresses the assembly manufacturing concerns as well as the additional handling operations such as shipping, burn-in, electrical test and SMT processing. The improvement specifically addresses the crack/gap phenomena by enhancing the area of the package where the damage has been observed – the top flange and corner areas (see Figure 2).

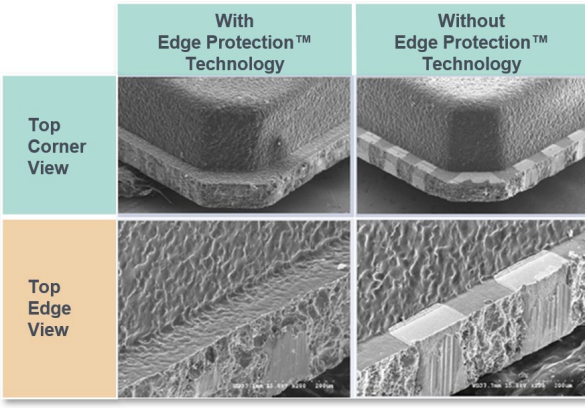

Figure 2 | Punch MLF® package – with and without Edge Protection™ technology applied to top flange and corner areas.

The Edge Protection technology solution has been developed with the constraint of not changing the existing device Package Outline Drawing, while increasing the strength of the flange and corner areas. The key to change with automotive devices is the magnitude of the impact to the targeted application. A significant change to the device bill of materials (BOM) can result in years of requalification effort on the part of the device manufacturer as well as the end automotive customer.

By modifying the mold chase, an extension of the mold compound is enabled to cover the top flange and corner areas. This 100-µm thick extension of the mold compound is formed on the top flange and corner areas of the package. These areas are not controlled by tolerances or dimensions, so the POD remains unaltered (see Figure 3).

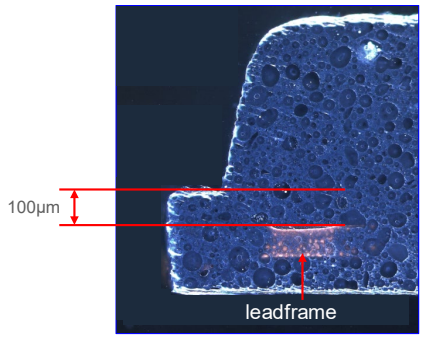

Figure 3 | Cross-section of punch MLF® device with Edge Protection™ technology applied to top flange area.

Providing an improvement that does not impact form, fit or function is an ideal condition for automotive end users, since those changes enable rapid implementation requiring limited effort and represent minimal risk to qualify and introduce. By meeting these criteria, enabling the Edge Protection technology for existing automotive punch MLF devices is a rather straightforward change.

The Edge Protection technology does not alter the POD for any defined critical dimensions and by design, the use of EPT does not impact any of the post assembly processes. This design approach also ensures that there is no impact to shipping medium such as tray designs, tape and reel pocket designs, burn-in/test sockets or SMT pick-and-place hardware. Since only the top flange and corner areas are affected by the mold compound extension, the impact to any of these post-assembly concerns is of minimal risk.

In practice, the implementation of the Edge Protection technology is virtually transparent to the end user. The exposed metal portions of the leadframe are no longer visible, but no other changes are visually apparent. An added benefit to implementing EPT and covering the top exposed lead area is that it minimizes the vision registration errors that may occur during the SMT process. This requires fewer alignment adjustments during device placement and achieves a higher throughput during the placement operation. In effect, eliminating the reflective surface of the device leads in the top flange area removes the opportunity for reflective and refractive vision placement errors that may occur during the SMT process (see Figure 4).

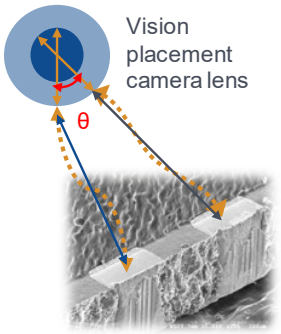

Figure 4 | Depiction of SMT vision system and reflective error correction for PCB alignment applied to compensate for the exposed lead surfaces of top flange area of a punch QFN without Edge Protection™ technology applied.

VALIDATING STRENGTH AND ROBUSTNESS TESTING

The improvement to the robustness of the punch MLF package when using EPT has been validated in simulation, actual use cases, test conditions and in laboratory evaluations. The Edge Protection technology has been in use with dual row MLF products since 2008. The technology was first used with the multi-row MLF package designs due to the thinner leadframe required by the etching manufacture process to form the interstitial lead design of the exterior and interior leads. The thin frame and interstitial design tend to make the leadframe more susceptible to damage during singulation and post-assembly processing. Since single row devices are inherently more robust due to a thicker leadframe material and leadframe design attributes, the EPT enhancement was added to further increase the package integrity for meeting the performance and reliability requirements of automotive applications.

Electrical testing of devices with the EPT enhancement has been supported within Amkor test facilities from 2008 - 2018. During this period, more than 500 million units of punch MLF devices of different body sizes and lead counts were electrically tested with no crack/gap incidents. Within the last 5-yrs, and in addition to the devices tested internally at Amkor, approximately 75 million devices with EPT were tested at customer test facilities without crack/gap issues.

In contrast, units without EPT tested during this period had reported incidents of crack/gap identified. Although the occurrences were infrequent, the need for improving the robustness of the punch MLF for test operations, including burn-in, was highlighted. As a result, a controlled laboratory study for implementing EPT on all punch MLF devices, both single-row and dual-row configurations, was initiated.

Prior to physical testing of the application of EPT to single-row punch MLF devices, a comprehensive modeling exercise was conducted to determine the stress point differences between a non-enhanced device and an EPT enhanced device. A 3-D model was generated of both configurations with the premise that all materials used in the package construction were linearly elastic (see Figure 5).

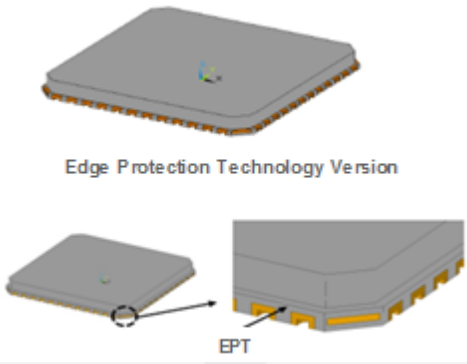

Figure 5 | Depiction of 3-D model of a punch MLF® with Edge Protection™ technology enhancement applied.

For the material properties used in the model, Amkor measured properties and supplier data were incorporated. The condition of pre-existing stress in the package was negated by process design, assuming the electrical mold compound (EMC) is basically stress free after post mold cure (PMC) of the applied condition of 175°C → 25°C.

The simulation focused on determining the stress differences between the non-enhanced device and the EPT device and predicting where points of stress would occur. The results of the simulation indicated that ~2x higher stress forces are required to induce a crack/gap on the device enhanced with EPT. The simulation also determined that the points of stress are different.

A laboratory-controlled evaluation of the effectiveness of EPT applied to punch MLF devices was conducted using 7-mm x 7-mm, 8-mm x 8-mm, and 10-mm x 10-mm single-row devices, with and without EMT. This same evaluation will be conducted on other body sizes when devices are available with the EPT enhancement applied.

An additional mechanical force simulation was conducted to determine the force required to form a micro-crack between the EMC and the leadframe interface. Defined as the initial stage of EMC to leadframe delamination, the micro-crack phenomena may or may not result in a breach of the package constructional integrity. However, the occurrence of a micro-crack does indicate that the interface has been weakened, having the potential to result in a device issue over time and cause further stress. In this evaluation a 5-mm x 5-mm – 16-lead package was used for the test vehicle.

As part of the mechanical force verification, a calibrated force ram was set for applying a force between pins 1 and 2 of the device under test (DUT) with a starting force of 500 gram force (gf). The force applied was increased in increments of 100 gf ranging from 500 – 1500 gf. The DUT was optically inspected using a 50x microscope for micro-cracking after each increment in force was applied. Any interface delamination noted was recorded as a micro-crack occurrence (see Figure 6). The results of the tests are discussed further in the next section.

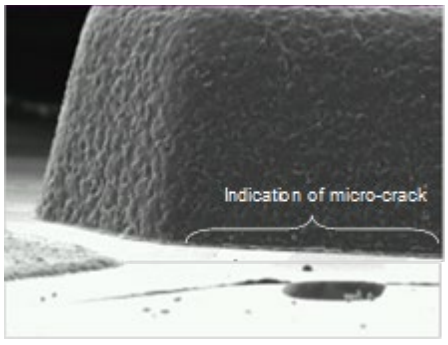

Figure 6 | Optical detection of micro-crack at 800 gf.

STRESS TESTING METHODS AND RESULTS

To validate the effectiveness of the EPT, a significant amount of time and effort was dedicated, starting with simulation and ending with physical data collection in laboratory evaluations and during electrical tests. In all cases, the data collected has shown that the EPT enhancement is effective and improves the robustness of the corner and side EMC to leadframe interface to resist crack/gap by a factor of ≥2x of a standard non-enhanced device. A review of all testing results follows.

SIMULATION RESULTS

The conclusions derived from the simulation was that the primary stress areas of the non-enhanced version and the EPT–enhanced version of the punch MLF occurred at different locations and that the EPT version is on average capable of sustaining 3x the stress on the flange area as the non-enhanced version (see Figure 7).

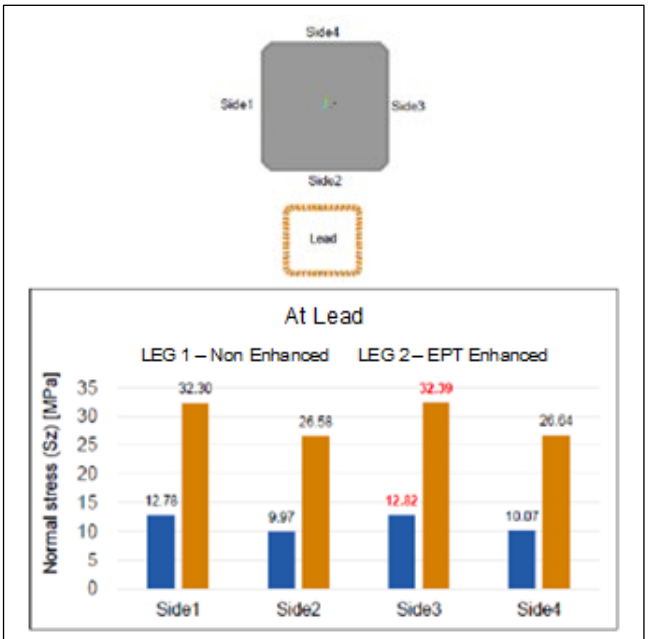

Figure 7 | Simulation stress results depicting improvement provided by Edge Protection™ technology.

EMPIRICAL MICRO-CRACK DATA RESULTS

Micro-cracks were the original reliability concern with the punch version of the MLF/QFN package format. In this test, the force was increased to 1500 gf to observe the effect of an extreme mechanical stress applied to the corner edge area. The results showed full separation and catastrophic failure of the EMC to leadframe interface. These types of severe delamination events have been observed during electrical test insertions of both burn-in and test handler contactor insertion (see Figure 8).

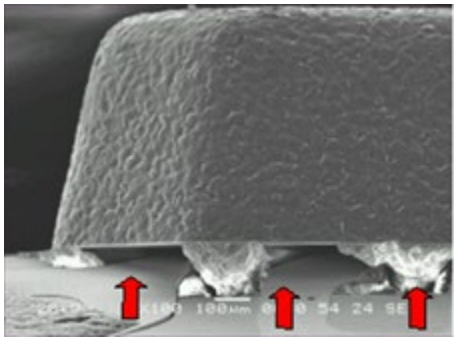

Figure 8 | Catastrophic failure of EMC to leadframe interface due to 1500-gf mechanical stress applied to the corner flange area.

LEADFRAME BEND TESTING RESULTS

To emulate potential assembly line handling issues that might result in crack/gap occurring on a device corner or side flange area, leadframes with and without EPT were subjected to extreme bending events by manual intervention.

In all instances of the bend testing for leadframes with the EPT enhancement, there were no cracks or gaps detected post singulation. For those leadframes without the EPT enhancement, cracks/gaps were detected before and after singulation, with the crack/gap between the top flange area and the leadframe or a crack on the bottom of the package, typically in the corner area. The collected data clearly indicates that leadframes with the EPT enhancement are much more robust and resistant to damage during assembly processing.

FORCE GAUGE TESTING RESULTS

The test results provided evidence that the minimum force required to cause a crack/gap in either the corner or side of a non-enhanced device is ~1000 gf or 9.8N. For the EPT-enhanced device, the minimum required force to cause a crack/gap was observed to be ~3250 gf or 31.85N for the corner flange area and 34.30N for the side flange area (see Figure 9).

LABORATORY MECHANICAL STRESS TESTING RESULTS

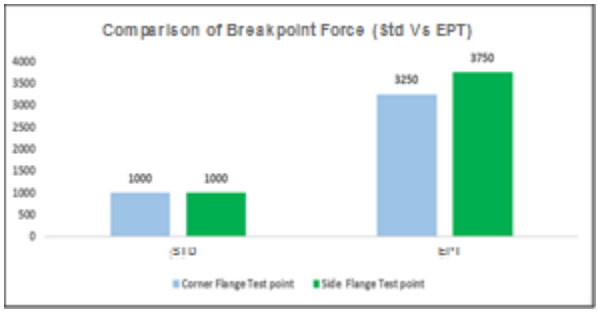

Figure 9 | Results from force gauge testing showing >3x improvement with Edge Protection™ technology applied.

The laboratory-controlled mechanical stress testing was conducted with custom designed fixturing and a repeatable process capable of producing accurate and credible results important for understanding the effectiveness of the EPT enhancement. Three different body sizes of the punch MLF package with and without the EPT enhancement were utilized in the testing.

The repeatability of the device performance for both the non-enhanced and EPT enhanced leadframe formats was demonstrated by the consistency in the load profiles collected during the testing. The load profiles collected when using the fixture were monitored with the use of computer software calibrated to detect unit deflection until a break was detected. The load profiles for the 8-mm x 8-mm devices with non-enhanced and EPT enhanced formats are shown in Figure 10.

Note that the deflection of the EPT enhanced versions started earlier and took much longer with greater force before reaching the break point. This provides further evidence of the effectiveness of the EPT.

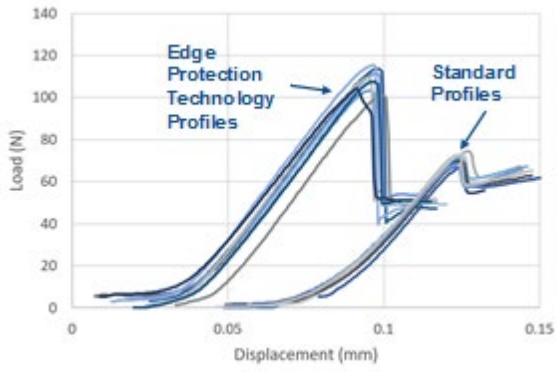

Figure 10 | Load profile curves depicting the resilience of the EPT enhancement – compared to the non-enhanced version, the EPT enhanced flange 'bends' but requires significantly more force to break.

From the data collected, regardless of the test method, the results were consistent within the test methodology applied. Further, the results of each test method demonstrated that the EPT-enabled devices, when compared to the non-enhanced version, showed a minimum 2x improvement to resisting mechanical damage due to mechanical stress.

As a result, it can be concluded that the application of EPT to the punch MLF package improves the robustness of the package and significantly reduces the risk of leadframe to EMC interface gaps/cracks. The consistency in the results, as well as the stated improvements, have been demonstrated through testing in four unique device body sizes as well in high volume manufacturing (HVM).

QUALITY IMPROVEMENT BENEFITS OF Edge Protection™ TECHNOLOGY

Multiple benefits are derived by implementing EPT, all representing improvements to quality and reliability of the punch MLF package:

1. significantly reducing the possibility of gaps/cracks resulting from mechanical stress
2. improving package robustness for all handling and processing steps
3. improving the package strength for burn-in and electrical ATE test insertions and
4. eliminating the incidents of SMT related issues.

Gaps/cracks have been observed to occur in the assembly operation as well as during electrical testing – burn-in and ATE functional testing (see Figure 11). The gap/crack that may result when sufficient mechanical stress is applied during these processing steps is difficult to detect using conventional methods. This is due to the fact that the typical gap/crack in the EMC/leadframe interface is not a total separation and the gap/crack occurs along the parting line of the interface making it difficult to detect using conventional optical inspection techniques or automated optical inspection (AOI) equipment. High magnification, ≥50x, is required to find the gap/cracks. In addition, since the EMC is black in color, the gap/cracks tend to blend in with the mold cap, appearing normal under typical lighting conditions.

Devices that are damaged during electrical testing have a high probability of not being detected during Final Visual Inspection (FVI) since the test operations are not typically equipped or trained to look for this phenomenon. Devices that are mechanically overstressed during the burn-in or electrical functional testing have been discovered after mounting on a PCB. These devices passed electrical testing but were detected after the PCB SMT reflow process.

The addition of the 100 µm of EMC has been demonstrated through thorough testing to provide a minimum of 2x improvement to the areas of the package that have proven to be sensitive to the gap/crack phenomena. As a result, the overall package quality is improved and the resistance to mechanical stress induced cracks/gaps in all process steps from assembly to the PCB mounting process is significantly improved as well. The containment and elimination of the gap/crack phenomena represents a significant overall improvement to the reliability performance of the punch MLF package. This improvement is especially important for demanding automotive applications where the devices may be exposed to harsh environmental conditions. The added protection is also important for automotive devices when considering the electrical testing the devices experience.

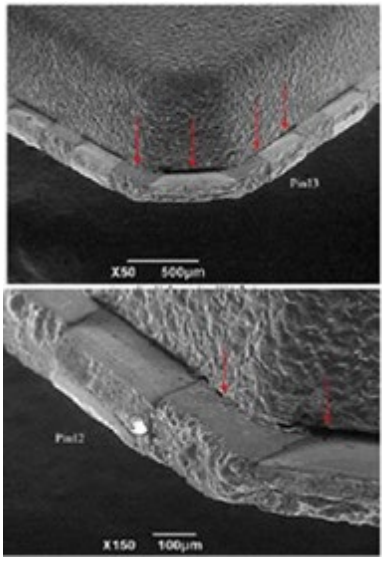

Figure 11 | Gap/crack confirmed to have been caused by excessive insertion force during electrical (ATE) testing.

A typical electrical test flow for an automotive device will include multiple test insertions, including burn-in and electrical functional testing at three temperatures – room (25°C), hot (125°C → 150°C), and cold (-40°C → -55°C). Additional stress from EMC expansion occurs during the PCB reflow process, increasing the risk of EMC to leadframe delamination if a crack/gap was formed at any of the processing steps prior to the SMT process.

CONCLUSIONS

The benefits of the Edge Protection technology have been extensively demonstrated both in laboratory testing as well as in actual practice. The test results have proven that EPT enables a minimum of 2x improvement of the punch MLF package to mechanical stress that can result in cranks/gaps of the EMC to leadframe interface.

The benefits extend beyond the assembly process and offer the same robust protection in the post-assembly handling processes such as burn-in and electrical ATE testing. This package level enhancement, enabled by a 100-µm thick mold cap extension over the expose top area of the

leadframe, will prevent the occurrences of cracks/gaps that have been reported in customer applications post SMT processing on PCBs.

Applying this technology is straightforward requiring no special equipment or additional processing steps. Enabling EPT for a given package body size of a punch MLF in assembly requires only a minor modification to the mold chase. There is no change to a device's Package Outline Drawing and no required change to test hardware – burn-in sockets or ATE contactors.

REFERENCES

[1] Marc A. Mangrum, "Edge Protection™ Technology for Punch MLF® Packaging"

[2] https://anysilicon.com/ultimate-guide-qfn-package/