Innovative Wafer Fan-out Technologies – Heterogeneous Integration for a Connected World

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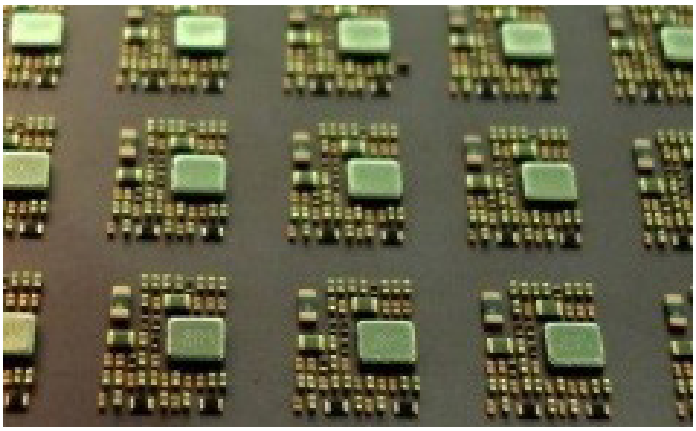
Abstract:

Advanced packaging technologies have increased in complexity over the years, transitioning from single to multi-die packaging, enabled by 3-dimensional (3D) integration, System in Package (SiP), Wafer Level Packaging (WLP), and increasingly creative approaches to embedding die. These new innovative packaging technologies enable more functionality and offer higher levels of integration within the same package footprint and often in an intensely reduced footprint. In fact, the latest advancements in heterogeneous integrated semiconductor packaging are able to provide reduced form-factor, increased data transfer rate and improved signal integrity and memory bandwidth, all with reduced power and improved thermal performance. In today's connected world with the proliferation of connected devices forcing continually higher system-level performance, semiconductor packaging has stepped up to play a pivotal role in providing solutions to the newest system-level requirements.

To further compound the semiconductor packaging challenge, the continued scaling of transistor geometries for semiconductor devices further increases the demand on next-level interconnect technologies. Heterogeneous integration of memory, logic, and power management devices is increasingly becoming the norm for next-generation mobile, high-performance graphics, and network applications. This requires advanced packaging technologies with capabilities for very high signal routing densities, efficient power distribution, and superior signal integrity. In addition, 3D package integration is often required, especially for mobile applications. This places an increased emphasis on the package technology's z-height reduction and thermal performance capabilities.

Traditional organic laminate substrates that utilize flip chip bonding have met the semiconductor industry's advanced interconnection needs for over 15 years.



With continued advancements in materials and processes, laminate substrates are expected to satisfy the majority of advanced package performance and cost requirements for years to come. However, feature-size limitations and electrical and thermal performance constraints will continue to restrict laminate substrates from meeting the integration requirements for next generation mobile and networking applications.

Emerging silicon-based interconnection technologies, such as through silicon via (TSV) have shown promise in this area. By leveraging the back end of line (BEOL) damascene processes of the wafer fab, multi-layer sub-micron signal trace densities can be achieved. However, supply chain limitations and intrinsic cost implications have limited the proliferation of 3D IC technology. In particular, for silicon interposers, there can be an undesirable effect to z-height and electrical performance due to the inherent thickness and parasitics of the silicon interposer.

This paper will discuss innovative wafer fan-out technologies that meet the heterogeneous integration requirements for an increasingly connected world, bridging the gap between organic laminate-based substrates and inorganic foundry-based silicon interconnect solutions.

1. Introduction

The continued scaling of transistor geometries for semiconductor devices and the need for heterogeneous integration of logic devices and high bandwidth memory (HBM) have been placing an increased demand on next- level interconnect technologies requiring very high routing densities and high electrical and thermal performance. Continuous miniaturization and 3D stacked multi-chip solutions with passive integration are required in the mobile and emerging Internet of Things (IoT)/ wearable markets. High-density fan-out (HDFO) packages can address these needs by incorporating the fine feature fabrication capabilities of wafer-level processing coupled with its ability to create 3D structures using through-mold interconnects such as tall copper (Cu) pillars and through package vias (TPVs) and advanced flip chip packaging technologies.

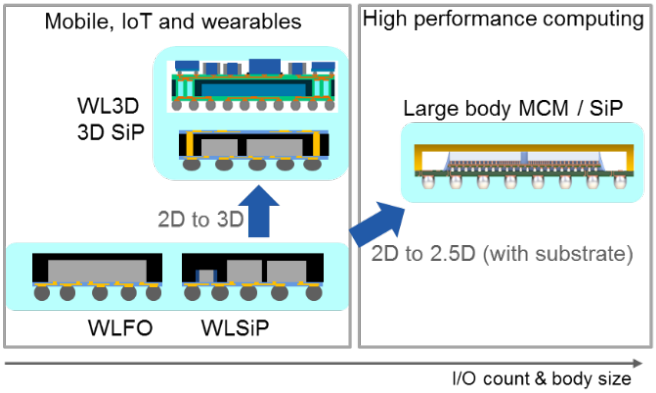


Figure 1: Fan-out package variants – from single-chip package to TSV-less 2.5D MCM package.

Figure 1 summarizes the representative package forms that can be implemented with fan-out technology. Various manufacturing methods for fan-out packages have been proposed, and some have already been applied to mass production using a redistribution layer (RDL). The Chip-first/RDL-last method is not dependent on solder joint for I/O to RDL interconnections, but there are restrictions on using various soldering based bumps and pad finishes. The RDL-first/Chip-last approach is suitable for complicated pattern fabrication and integration of various forms of active chips and passive components. Moreover, it has advantages for efficient yield and cycle time management since the RDL formation process and the chip assembly process are managed separately.

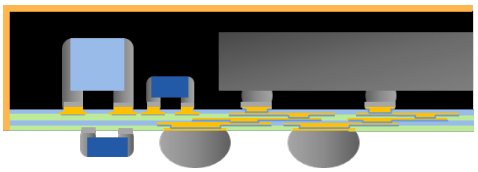
In addition to the existing Chip-first fan-out method, Amkor has developed an innovative Chip-last fan-out technology called Silicon Wafer Integrated Fan-out Technology (SWIFT®) packaging [1]. SWIFT technology was originally developed for the mobile market. As its robustness and excellent scalability has been confirmed, the technology is extending into large body multi-die products and proposed as an alternative to the 2.5D integration with a TSV interposer.

To support a growing variety of customer needs in a timely manner, it is necessary to have a more flexible package portfolio and to create new technology toolboxes. Furthermore, combining them as necessary into final package constructions is also a key element in Amkor's fan-out technology development.

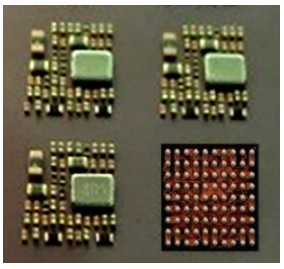
2. Innovative Wafer Fan-Out Technologies

WLSiP

The challenges with the conventional System in Package (SiP) approach using printed circuit boards (PCBs) are its limited scalability for fabricating fine line/space trace circuits and capability for reducing package thickness. More complicated system integration and further miniaturization can be realized with HDFO technology. Figure 2 (a) illustrates the structure of a representative Wafer Level System-in-Package (WLSiP) that can be built with a Chip-last HDFO approach such as SWIFT technology. Active device and passive component are assembled and embedded in the mold. Fan-out wafer level packaging (FOWLP) is also capable of conformal shielding, which is increasingly requested for SiP modules. Significant area optimization and package profile reduction can be accomplished by using fine feature redistribution layer metal and design optimization. Figure 2 (b) shows an example of an 8 x 8 mm^2 size WLSiP module processed with Chip-first fan-out technology.



(a)



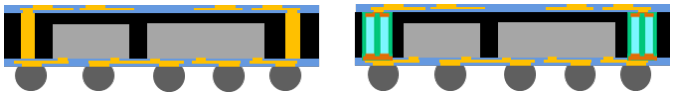
(b)

Figure 2: WLSiP integration with fan-out technology: (a) representative cross-section structure of WLSiP; and (b) top down view of 8 x 8 mm^2 WLSiP sample.

There is no constraint on the surface finish type of passive components and package or I/O type of the active chip with Chip-last HDFO approach such as SWIFT packaging because the RDL process is performed before the active devices and passive components are assembled.

WL3D

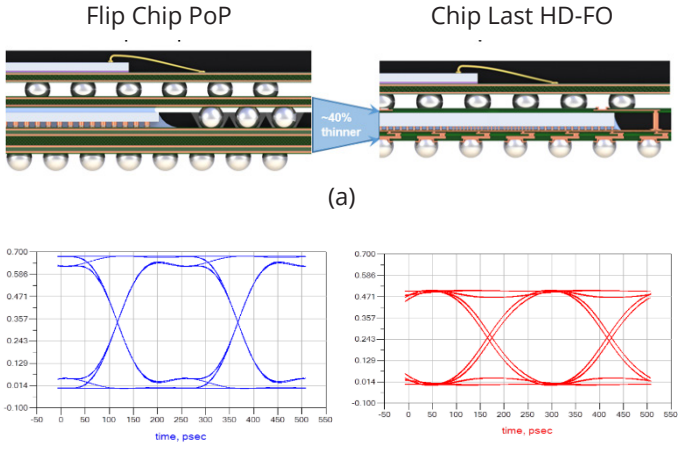
The flexibility of the Chip-last HDFO package structure offers benefits for creating 3D assemblies. Tall copper (Cu) pillars and TPV can be used to create vertical integration which enables 3D structures where a package can be stacked on top of the bottom HDFO or additional active die and passive components can be mounted and then embedded in the mold (Figure 3).



(a) (b)

Figure 3: 3D PoP fan-out design with dual die structure with top side RDL: (a) tall Cu pillars for vertical interconnect; and (b) TPV used for vertical interconnect.

Figure 4 (a) shows cross-section representations of the laminated-substrate based flip chip PoP and the equivalent SWIFT® PoP structures used for a comparison study. The SWIFT package for this PoP structure results in a thickness of 390 µm – a 40% reduction in overall bottom package thickness. SWIFT technology exhibits enhanced electrical signal integrity, superior impedance matching, optimized power distribution, and improved thermal performance compared to the flip chip PoP. The eye diagram comparison at 4 Gbps can be seen in Figure 4 (b).



(a)

(b)

Fig. 4: WL3D PoP comparison. (a) Package thickness comparison with cross-sectional view (b) Comparison of eye diagrams at 4 Gbps.

Large Body MCM

Pioneering 2.5D ICs which have HBM and logic mounted side by side on a silicon (Si) interposer with TSVs have been in volume production for graphics processing units (GPUs) and field programmable gate arrays (FPGAs). However, challenges such as supply chain limitations and increased cost have limited the proliferation of 2.5D/3D IC technology. Due to the I/O insertion loss caused by the TSV [2], more stringent electrical requirements for high-speed performance are pushing some next-generation network/server products in the direction of a TSV-less construction with 2.5D.

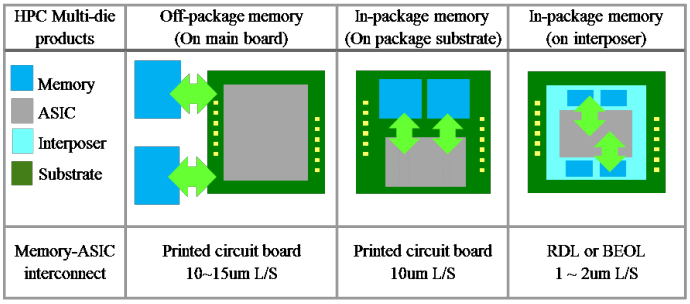
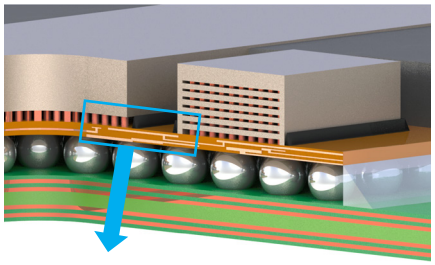
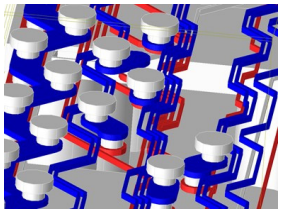


Fig. 5: ASIC and memory integration trends in high performance computing (HPC) applications.

SWIFT packaging is a TSV-less solution using HDFO technology. An HBM that requires a 1024-bit interface can be routed in SWIFT technology with acceptable signal integrity using several different approaches, one of which is shown in Figure 6, using mixed signal and ground traces. Both multiple layers of RDL with organic passivation and a combination of the RDL and back end of line (BEOL) Cu can be used to route HBM. Line and space required to realize this is 2 µm or smaller.



(a)



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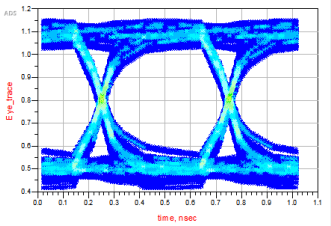

(c)

Fig. 6: HDFO integration of ASIC and HBM: (a) Illustration of a SWIFT® module attached to a package substrate, (b) Trace routing with 2-µm line/space RDL, and (c) Simulated eye diagram with all signals active.

HDFO Technology Toolboxes

High-density system integration capabilities can be extended by creating new toolboxes with fan-out technology and by improving current capabilities to the next level [3]. Several key technology toolboxes are shown in Table 1.

Conclusion

Heterogeneous system integration capabilities of the fan-out technology can be further extended to WLSiP, WL3D and large-body MCM packages by using advanced HDFO coupled with newly created and improved technology toolboxes. Highly versatile and high-performance packaging approaches like SWIFT technology are the key for achieving advanced packaging success for next generation mobile, IoT and high-performance computing applications.

Table 1: HDFO Technology Toolboxes

Item	Requirements
Active device	Die and package interconnect to RDL with & without bump on I/O
Passive component	Embedding or surface mount of low-profile passives and integrated passive devices IPDs with various terminal finishes
RDL	Single or dual-side RDL with fine line/space capability (≤2 µm) and optimized routing design
Vertical connection	Allows dual-side RDL and 3D package and die stacking
Wafer molding	Molded underfill tightens die to die & die to component design rules
Fan-out module attach to substrate	Attachment of fan-out module to substrate with good reliability and controlled warpage

Acknowledgment

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