

Package assembly design kits bring value to semiconductor designs

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Today's state-of-the-art packaging designs allow semiconductor companies and their customers to implement the latest technologies and deliver the "wow-factor" with an ever-increasing number of features and options in space-constrained form factors. Other system constraints include: time to market, design cycle time, accuracy, productivity and more.

To simplify the design of the newest advanced packages, such as high-density fan-out (HDFO) and to address all these other constraints, Amkor has introduced the SmartPackage™ Package Assembly Design Kit (PADK). This article will discuss the need and value of such design kits.

The value of design kits

Semiconductor and integrated circuit (IC) designers have used process design kits (PDKs) for decades to achieve design for manufacturability (DfM). These foundry-specific PDKs are used with electronic design automation (EDA) tools in the chip design process. These checks are known by IC designers as layout vs. schematic (LVS) and layout vs. layout (LVL) – terms that are not used in the packaging world.

For outsourced semiconductor assembly and test suppliers (OSATS), package designs have relied on verification methods such as design rule checks (DRC) in computer-aided design (CAD) software and other EDA verification methods such as computer-aided manufacturing (CAM) checks. The combination of these checks ensures that each package design meets the intended manufacturing and assembly requirements.

Adding packaging to the PDK methodology

As die and package integration complexity continues to increase with 2.5D and 3D structures, so does the need to integrate a die- and package-level verification process – basically, it is the integration of the PDK in IC design and DRC and CAM checks in advanced packaging. An example

of this advanced package complexity with redistribution layers (RDLs), vias, interposers, and more is shown in **Figure 1**.

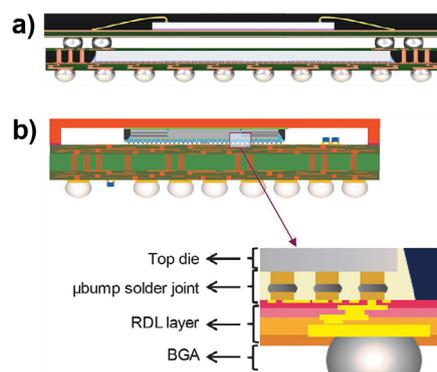


Figure 1: HDFO package-on-package (PoP) structures showing a) tall copper pillars on both the right- and left-hand sides; and b) an HDFO cross section.

The newest advanced packaging designs, such as high-density fan-out, are at the intersection of the IC design world and the packaging design world. Because PDKs have been used in IC design for many years, they provide an established approach for advanced packages as well. Taking tools that were used exclusively for IC design and applying them to package design creates a bridge between the two domains.

Gerber data is the de facto standard used for exchanging data in the printed circuit board industry and is the typical packaging design export for artwork generation. In contrast, the de facto industry standard for IC designs export is GDSII for data exchange of ICs and

IC layouts. For HDFO packaging, where the final layers are actually semiconductor-type processes, the GDSII data is essential and a natural extension for design data transfer and provides the best of both worlds.

The existing package design approach is shown in **Figure 2**. Once the user selects a specific package, the packaging supplier provides the design rules. Each customer has their own design database setup where they adapt the package design rules to their specific database configuration. The number of iterations and length of time to resolve these rules have always been an issue in the traditional package verification process. For today's HDFO package designs, this approach no longer works.

To fill the void between die design and package design, Amkor's SmartPackage PADK brings together design, manufacturing, and assembly for HDFO packages. Although IC designers are aware of the process and advantages of PDKs to conduct LVL/LVS verification, they have limited knowledge of package design and package design tool DRC/CAM verification processes. While PADKs offer similar advantages to PDKs, there are some distinct differences in how they are implemented. One of the critical, and often forgotten or neglected, aspects of the traditional process is that packaging engineers are normally not completely familiar with the IC design process. The same is also true in that IC designers are normally not completely familiar with

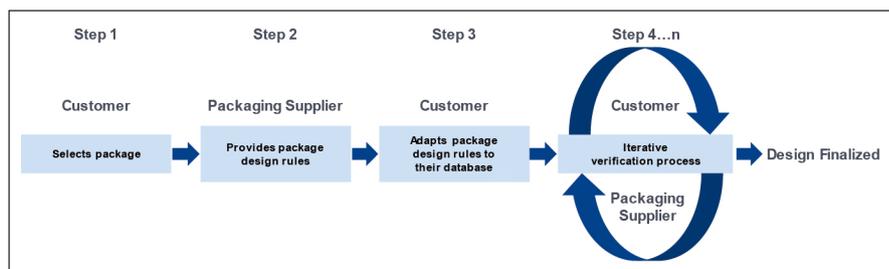


Figure 2: The traditional package verification process.

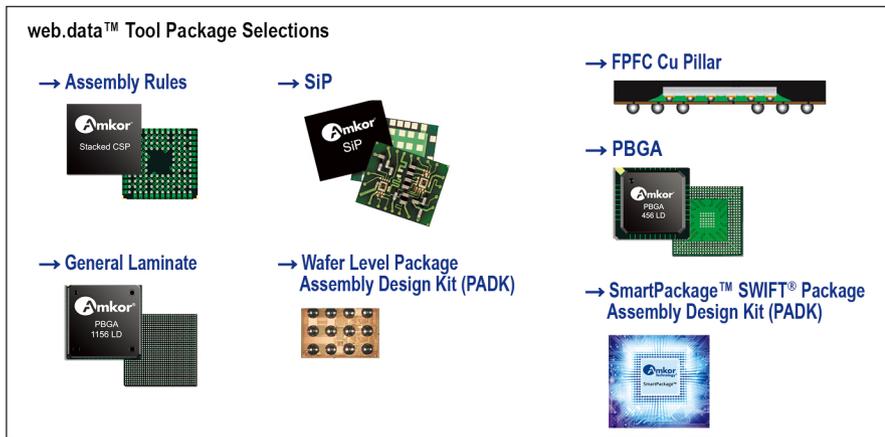


Figure 3: User accessible documents in the SmartPackage PADK.

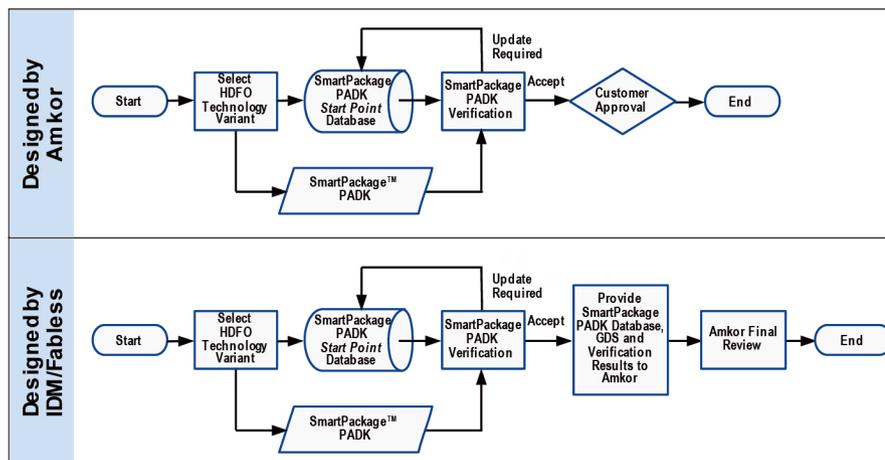


Figure 4: The PADK package verification process.

the package design process. This has created the “perfect storm” as HDFO is at the intersection of the IC design world and the packaging design world.

Getting packaging details right

SmartPackage PADKs are designed to ensure that the customer’s HDFO design meets Amkor’s design and assembly requirements throughout the design phase. With this tool, there is no guessing whether the proper design rules have been followed. From 3D interconnect, 3D alignment, feature size and routing, the PADK provides an easy to use method to gain greater control and ensure a complete and swift design verification in one pass. SmartPackage PADK verification examples include:

- Pin alignment (die to package);
- Feature size design rule validation;
- Die and component placement design rule validation; and
- Netlist connectivity.

To utilize the SmartPackage PADK, customers are required to use the Amkor Start Point database. This database has all the layer structures, layer classes and subclasses, pad stacks, and essentially all the design rules a customer needs to get started on their design. In the IC world, if the foundry does not provide the database, the IC design house must establish it – which is a long and tedious process. For packaging, Amkor has invested time and effort to develop a Start Point database for customers.

For the new PADK approach, users do not have to be familiar with the previous package design process. The new approach makes it easy to obtain the knowledge to implement the new methodology in a very easy to use, straightforward manner. The goal is to get the design attribute outputs from whatever EDA tool they currently use into Mentor’s Calibre™ system. Once inside of Calibre, Mentor has plenty of high-density advanced packaging (HDAP)

tools to ensure a complete and trustworthy verification. The next section provides more details on this partnership and the tools made available to Amkor’s PADK users.

Once designed in the package design software, the customer exports the manufacturing outputs that are conditioned by the Start Point database and the outputs are verified in Calibre. Beyond traditional packaging items like trace/space and via sizes, the PADK will also check component spacing and perform many assembly and manufacturing checks, thereby building on the strengths of the package design software and making it a much more powerful instrument than just a traditional package design checking software tool.

For a new user to access the Amkor PADK, the user must request access via the Amkor Account Team. When a PADK is revised, customers that have access to the PADK will receive an update notification. After access is approved, the user sees a list of documents available to them as shown in **Figure 3**. By selecting the desired PADK, the user is presented with a nondisclosure agreement (NDA). Once the NDA is accepted, the user can download the PADK. The SmartPackage PADK contains: 1) Design rules document; 2) Calibre rule deck; 3) Required configuration and instructional information; and 4) Start Point design database.

As shown in **Figure 4**, the Start Point database is a package design database that has been developed for customers to use on their HDFO designs. It allows them to “get up and running” after simply inputting a few minor details. The process is not quite the same as the traditional PDK or the traditional packaging approach, so awareness of these differences is important.

In traditional IC designs, designers have very little discretion. On the other hand, with laminate package design tools, designers have a lot of discretion. They are able to manipulate the design rules. The PADK is a process that can be used “on the fly” to bring the customer in-line with packaging assembly processes and prevent them from straying from approved rules.

PADK and Mentor’s HDAP design process and tools

In 2018, Amkor and Mentor jointly announced the industry’s first partnership to support Mentor’s high-density advanced packaging (HDAP) design process and tools. Amkor’s SmartPackage PADK takes advantage of Mentor’s HDAP design process and industry-leading tools.

Results from PADKs

One of the important user benefits of the PADK is that when it detects an error, the error is flagged as a design error. The PADK identifies the design rule, so the designer can refer to the SmartPackage design rules and see the violation or value discrepancy. This straightforward, intuitive process is receiving considerable interest from users and potential users. Surprisingly, they usually have all the tools – but this is an aspect of which they have not previously taken advantage. So, it takes training, knowledge transfer, and establishing trust in the packaging-level partnership to take this next step.

Some of the most commonly encountered verification issues that the PADK tool highlights include:

1. Component placement/floor planning issues;
2. Die-to-die spacing;
3. Capacitor-to-die spacing;
4. Feature-to-feature spacing; and
5. Feature size deviation.

Figure 5 shows the type of error a user might encounter.



Figure 5: Example of a design rule check violation for component spacing.

Using the new PADK, users have already demonstrated that an extreme cycle time reduction for HDFO packages is possible. A major time reduction occurs by reducing the iteration cycles between the user and the package supplier as shown in Figure 2. This reduction can be from days or even weeks, to only a few minutes. The process allows users to get to the desired state in their design, run their check, fix the errors and get back to designing again before they get too far into the design process only to realize they were headed in the wrong direction.

Because users can perform the verification in real-time in their facility, when the design is sent to Amkor, it will be easily accepted and can efficiently progress towards production. By identifying and correcting the errors themselves, users have found the new process to be much more flexible than the old way because it allows them to: 1) prioritize revisions, 2) realize more of the goals they wanted to achieve in the design, and 3) better understand the intuition/methodology behind the rules. This educational process also helps them in future designs to avoid and resolve problems even faster.

Towards faster time to market and more

In the packaging world, the situation is quite different because there are many different ways to achieve the same goals by modifying different rules and compensating for changes in other locations. To avoid problems from this “too flexible,” laissez-faire approach, the SmartPackage PADK moves toward the IC design methodology to stay within more stringent requirements for multi-layer packages.

Towards faster time to market and more

IC designs tend to be very static, so the rules must be followed without deviation. In the packaging world, the situation is quite different because there are many different ways to achieve the same goals by modifying different rules and compensating for changes in other locations. To avoid problems from this “too flexible,” laissez-faire approach, the SmartPackage PADK moves toward the IC design methodology to stay within more stringent requirements for multi-layer packages.

For users, the PADK methodology leverages existing design tool capabilities by utilizing the investment they have already made and provides enhancements to simplify and speed up the design verification process for packaging. The results are early, rapid and accurate verification of advanced packages to significantly increase productivity, reduce cycle times and limit the number of design iterations.

Acknowledgement

SmartPackage is a trademark of Amkor Technology, Inc. Calibre is a trademark of Mentor.

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