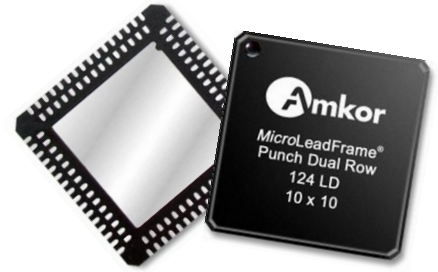




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# AN3015

## Surface Mount Guidelines for Amkor Dual Row *MicroLeadFrame*® (DRMLF®)

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## Introduction

This application note provides guidelines for surface mount technology (SMT) assembly of Amkor's Dual Row *MicroLeadFrame*® packages (DRMLF®) using prevalent practices in the SMT industry and standards such as IPC and JEDEC. It includes recommendations for printed-circuit board (PCB) land pad design, stencil design, mounting, reflow profile and rework processes.

## Scope

This application note serves only as general guidelines to help users with a starting point. Further study and development efforts may be needed by the users to optimize the design and processes for their specific device application, surface mount practices and requirements.

This document applies to various Amkor DRMLF package sizes with standard lead pitch of 0.50 to 0.65 mm.

## Package Description

The DRMLF is an extension to the standard single row *MicroLeadFrame* (MLF®) where electrical contact to the PCB is made by soldering an additional row of leads on bottom of the package. Like MLF, it is a near CSP plastic encapsulated package with a copper lead frame substrate. Amkor's ePad technology enhances the thermal and electrical properties of the package. The exposed die attach paddle on the bottom is designed to be soldered to PCB for efficient heat conduction and a stable ground.

MLF and DRMLF are also known as quad-flat no-leads (QFN) and dual-quad-flat no-leads (DQFN) respectively, in semiconductor packaging and SMT industry.

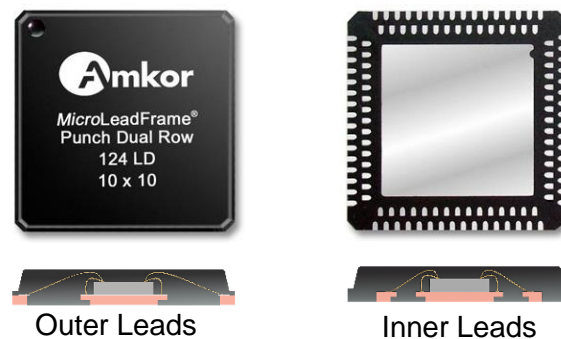


Figure 1. Dual Row MLF® Package Photo and Cross Section Drawings

## Surface Mount Considerations for DRMLF Package

Several primary factors that can affect the mounting of the package on the board:

- PCB land pad and via design
- PCB flatness
- PCB pad finish
- Package lead finish
- Stencil design
- Solder paste type and depositing volume

- Mounting (pick & place) capability
- Reflow profile

## PCB Design Guidelines

Figure 2 shows the typical dimensions required to develop a PCB land pattern based on IPC-7351 conventions. Refer to the specific package outline drawing for the values. Note that actual package outline drawings do not describe the S2 or S3 dimension and values must be calculated by the designer.

Refer to guidelines in IPC-7093 Design and Assembly Process Implementation for Bottom Termination Components.

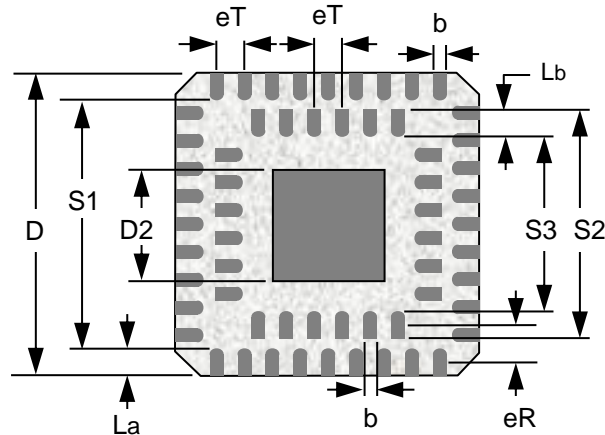
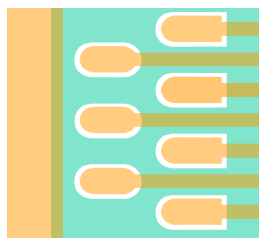


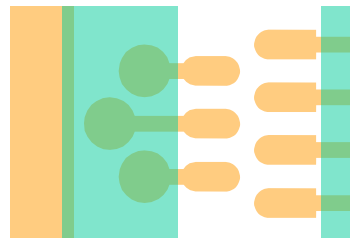
Figure 2. DRMLF® Dimensions for PCB Land Pad Design

## Perimeter Land Pad

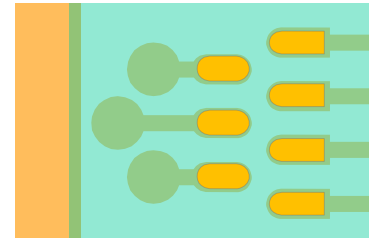
- Non-solder mask-defined (NSMD) pad is recommended for inner and outer row lands  $\geq 0.500$  mm pitch.
- For package pitches  $< 0.500$  mm and/or where NSMD pads can't be done reliably, a single large solder mask opening "trench" is a preferred design over solder mask-defined (SMD) pads.



Non-Solder Mask-defined (NSMD) for Pitch  $\geq 0.500$  mm



Large Solder Mask Opening (Trench) for Pitch  $< 0.500$  mm



Solder Mask-defined (SMD), 2<sup>nd</sup> option for Pitch  $< 0.500$

Figure 3. Recommended Solder Mask for Perimeter Pads

- Refer to the specific package outline drawing for information and dimensions to aid in land pad design.
- Table 1 lists few important factors to consider for designing the land pads. Table 2 is summary of recommended land pad sizes for few Amkor's DRMLF® packages. Figure 5 depicts a generic land pad layout for DRMLF.

Table 1. Factors to Consider for Land Pad Design

<b>SMT Placement Accuracy</b>	$\pm 0.0250$ mm ( $\pm 0.050$ mm typical)
<b>Toe Fillet (<math>J_{To}</math>), Outer Row Pad</b>	$\geq 0.150$ mm (for exposed lead end/flank) $\geq 0.400$ mm (for wettable lead end/flank) <sup>(1)</sup>
<b>Toe Fillet (<math>J_{Ti}</math>), Inner Row Pad</b>	$0.050 - 0.080$ mm <sup>(2)</sup>
<b>Heel Fillet (<math>J_H</math>), Inner/Outer Row Pads</b>	$\geq 0.050$ mm <sup>(2)</sup>
<b>Side Fillet (<math>J_S</math>)</b>	$\geq 0.000$ mm
<b>Land to Land Spacing (<math>C_{LL}</math>)</b>	$\geq 0.200$ mm
<b>NSMD Clearance to Pad (<math>C_{SM}</math>)</b>	$\geq 0.050$ mm (preferred $0.060 - 0.075$ mm)
<b>NSMD Web Between Pads (Web)</b>	$\geq 0.075$ mm (preferred more than $0.100$ mm)
<b>Land Width, Inner/Outer Rows (<math>X</math>)</b>	$\geq$ Package nominal pad width ( $b$ ); $\leq 0.370$ mm f/0.650 pitch, $0.280$ mm f/0.500 pitch, $0.225$ mm f/0.400 pitch
<b>Land Length, Inner &amp; Outer Rows (<math>Y1</math> &amp; <math>Y2</math>)</b>	Table 2
<b>Thermal Pad to Land Spacing (<math>C_{PL}</math>)</b>	$\geq 0.200$ mm
<b>SMD Thermal Pad Opening</b>	1:1 Package ePad
<b>SMD Overlap</b>	$\geq 0.050$ mm
<b>Silk Screen</b>	None, under package body (can cause assembly defect)

(1) Need longer land extended outward from edge of the package with wettable lead end/flank, for best (Automatic Optical Inspection) inspectable fillet formation.

(2) Providing min.  $C_{LL}$  and  $C_{PL}$  are maintained.

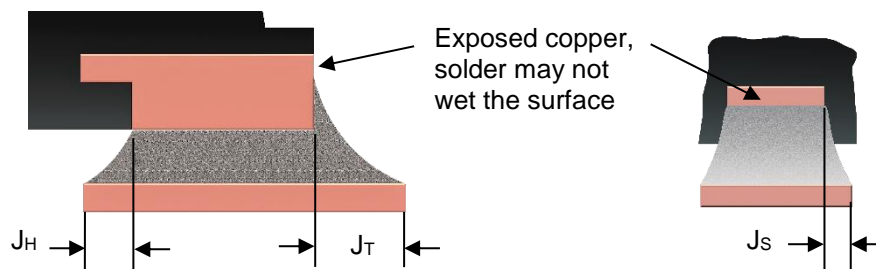


Figure 4: IPC Definition of Toe, Heel and Side Fillets

Table 2. Recommended Land Pad Dimensions by Package Type

Package Attributes and Dimensions						PCB Land Pad Dimensions					
DRMLF® Package Size	I/O	Lead Pitch (eT)	Row Pitch (eR)	b (nom)	L (nom)	X (min)	X (max)	Y1 (min)	Y1 (max) <sup>(1)</sup>	Y2 (min)	Y2 (max)
8 x 8	76	0.60	0.70	0.20	0.40	0.25	0.28	0.60	0.90	0.50	0.56
8 x 8	92, 100	0.50	0.65	0.22	0.40	0.25	0.28	0.60	0.90	0.50	0.56
9 x 9	84	0.65	0.75	0.22	0.40	0.25	0.37	0.60	0.90	0.50	0.56
9 x 9	108, 116	0.50	0.65	0.22	0.40	0.25	0.28	0.60	0.90	0.50	0.56
10 x 10	100	0.65	0.75	0.22	0.40	0.25	0.37	0.60	0.90	0.50	0.56
10 x 10	124, 132	0.50	0.65	0.22	0.40	0.25	0.28	0.60	0.90	0.50	0.56
11 x 11	132, 144 148	0.50	0.65	0.22	0.40	0.25	0.28	0.60	0.90	0.50	0.56
12 x 12	124	0.65	0.75	0.22	0.40	0.25	0.37	0.60	0.90	0.50	0.56
12 x 12	156, 164	0.50	0.65	0.22	0.40	0.25	0.28	0.60	0.90	0.50	0.56
13 x 13	164	0.50	0.58	0.25	0.35	0.25	0.28	0.55	0.90	0.45	0.51
13 x 13	164, 172	0.50	0.65	0.22	0.40	0.25	0.28	0.60	0.90	0.50	0.56

All dimensions are in mm

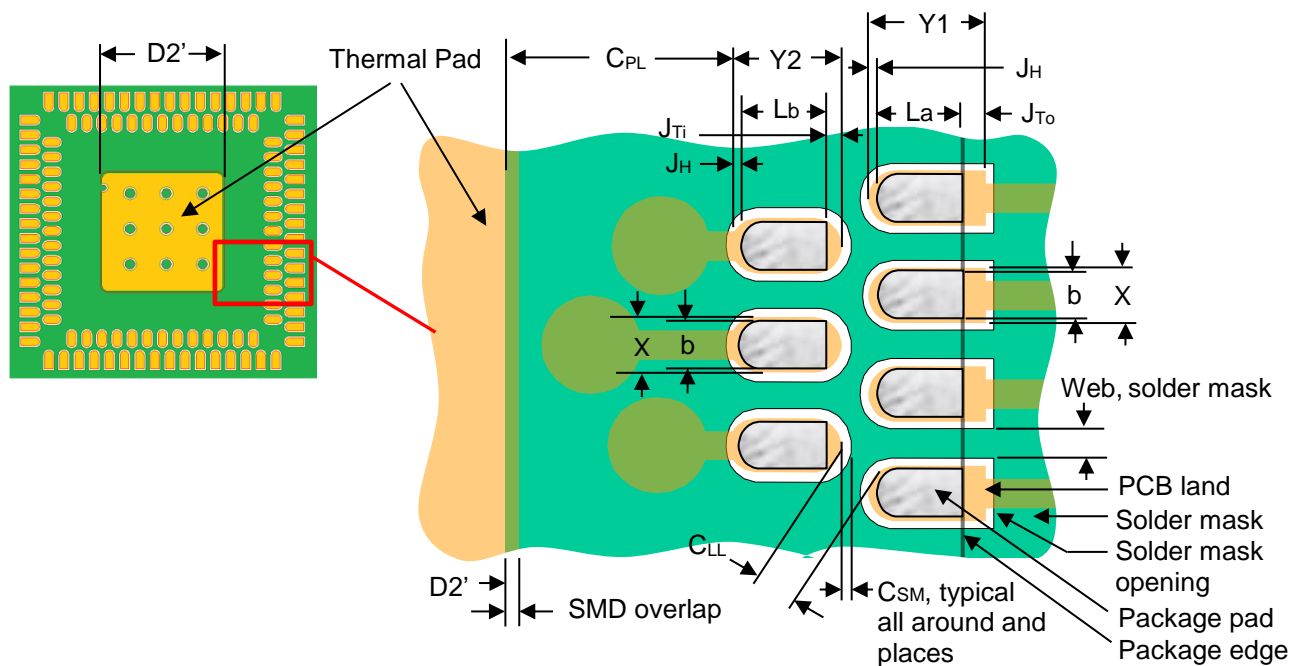


Figure 5. Land Pattern Design for DRMLF®

## Exposed (Center) Thermal/Electrical Pad and Via

If application requires effective electrical connection and/or conduction of heat through dielectric layers of PCB, thermal pad and vias are need (Figure 6):

Thermal pad, preferably, defined by the solder mask (SMD) and should match the size of the ePad of the component.

- Solder mask (SMD) to overlap thermal pad minimum 0.050 mm.
- Minimum 0.200 mm thermal pad to land clearance (C<sub>PL</sub>) is necessary to prevent solder shorts, for most designs.
- Number of thermal vias will depend on the power dissipation and electrical requirements. Experience and simulations from standard single row MLF<sup>®</sup> can be considered. Figure 6 shows the effect of number of vias on  $\Theta_{ja}$  plotted for a 7 x 7mm, 48 lead package, as an example.

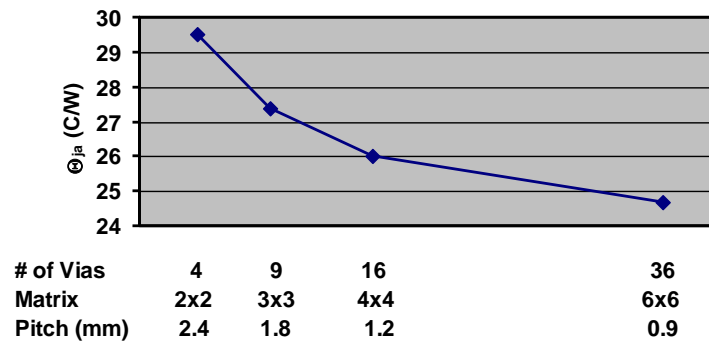


Figure 6. Effect of Number of Thermal Via on Package Thermal Performance

- Thermal vias can be placed at approximately 1.0-1.2 mm pitch with via drill diameter of 0.2-0.3 mm.
- Thermal via should be solid (no thermal relief web or spoke connections).
- Thermal vias must be filled, plugged or capped to prevent solder loss from protrusions – smaller diameter vias are easier to fill or cap.
- Solder mask tenting the vias from the top side of PCB is the recommended method to minimize voids in the thermal pad area solder connection that can affect thermal performance.

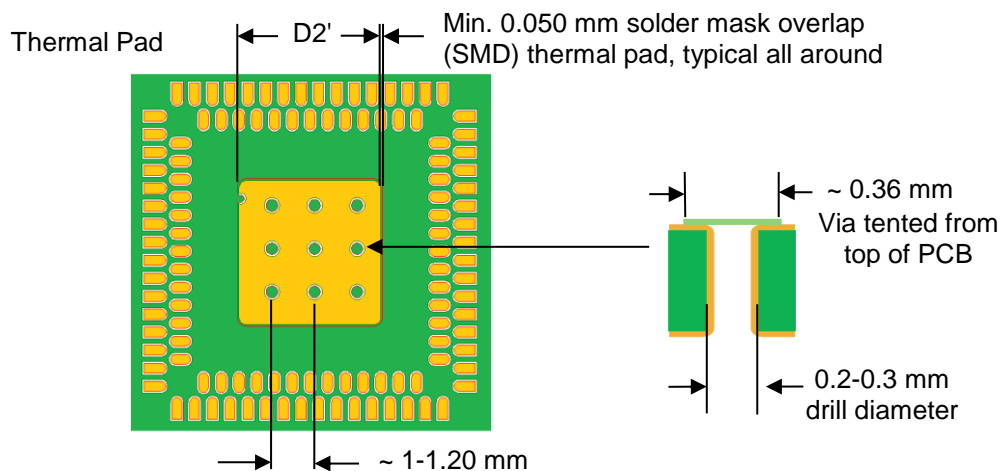


Figure 7. MLF<sup>®</sup> Thermal Pad and Via Design

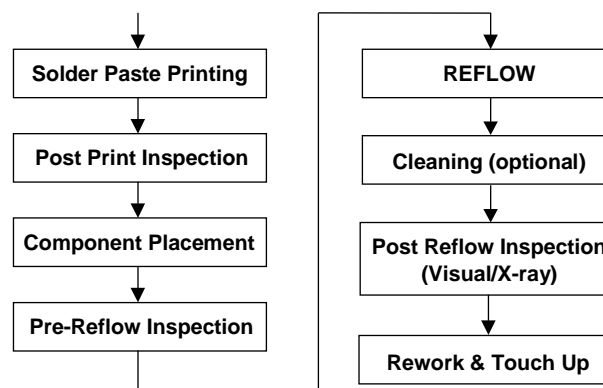
## PCB Pad Surface Finish

Below pad finishes are compatible with DRMLF:

- Organic solderability protectant (OSP)
- Electroless nickel immersion gold (ENIG)
- Immersion Sn
- Immersion Ag
- Hot air solder leveled (HASL) – not recommended due to uneven surface finish

## Board Assembly

Below is a typical SMT assembly process flow to mount DRMLF® to PCB.



**Figure 8. Typical SMT Assembly Process Flow**

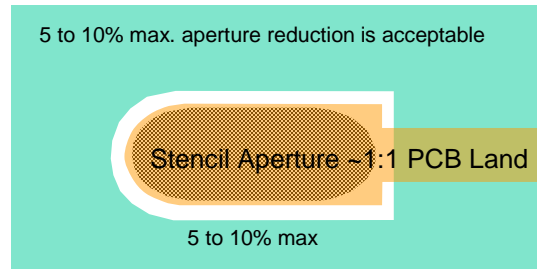
Because of the DRMLF low stand-off, small pitch, double row flat lead surface, large thermal pad underneath the package and its proximity to the inner row leads, extra care needed for process development and control during assembly.

- DRMLF is more sensitive to PCB warpage and board/pad flatness – mind the condition throughout the assembly and rework processes.
- Uniform printed solder paste height and volume pad to pad on perimeter lands are necessary.
- Component placement down force/z-height is critical – set to drive component leads half way into the solder paste height/thickness. Too low or excessive drive can cause component floating, tilt, misalignment and/or paste displacement (squeeze out) that can result in solder open and/or short.
- Solder joint standoff height of ~50 to 75  $\mu\text{m}$  with good fillet on outside toe as a minimum produce a more reliable, longer life joints. Lower standoff can cause a higher chance for solder short on inner pads.
- Solder voids in thermal pads are common and can affect thermal performance. Excessively number or poorly made thermal vias, high paste flux volume and/or poor reflow profile can all cause excessive void.
- Water-soluble flux and cleaning process is not recommended because of low clearance. However, cleaning improves with increase in stand-off height and using “trench” solder mask for the PCB land pad design.

## Stencil Design

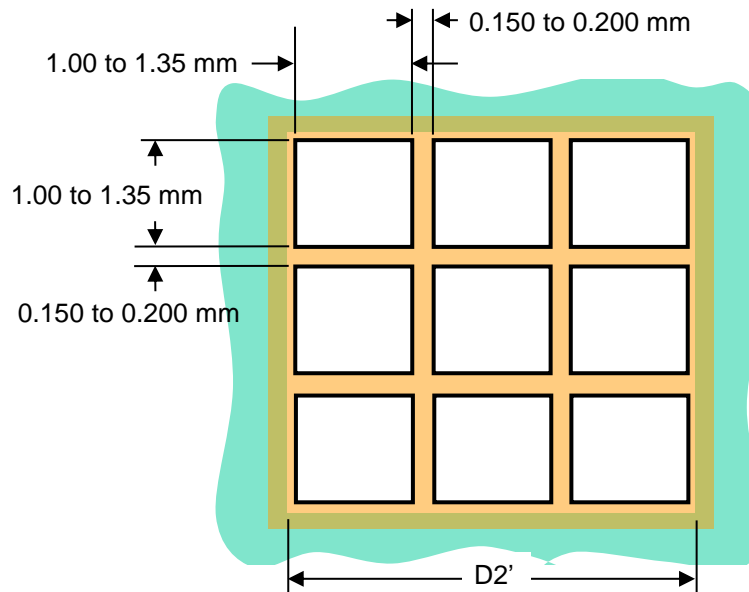
Stencil foil should be stainless steel and laser cut with electro polished apertures or better.

- Stencil foil thickness should be 1.00 to 0.125 mm for higher component standoff.
- Aperture area ratios  $\geq 0.66$  and aspect ratios  $\geq 1.5$ .
- Aperture size for perimeter inner and outer rows should be near 1:1 to PCB pads. A 5 to 10% max. aperture reduction is acceptable, only if needed to account for mounting and PCB tolerances (Figure 8).



**Figure 8. Stencil Aperture Design for Perimeter Pad**

- Aperture opening for thermal pad should be approximately 0.75:1 to PCB pad, using a hatch pattern to support outgassing of flux and other volatiles from PCB during reflow (Figure 9). This will help to prevent floating of the DRMLF<sup>®</sup>, minimize solder void and spattering.



**Figure 9. Stencil Aperture Design for Thermal Pad**

## Solder Paste

Solder paste selection is normally driven by application and overall assembly requirement. In general, a “No Clean” lead-free Sn-Ag-Cu (SAC) solder paste type 3 or 4 is recommended for mounting DRMLF<sup>®</sup> packages.



## Placement

A typical SMT pick and place machine equipped with vision-alignment system accuracy of  $\pm 0.050$  mm or better can mount the DRMLF, same as similar pitch BGAs.

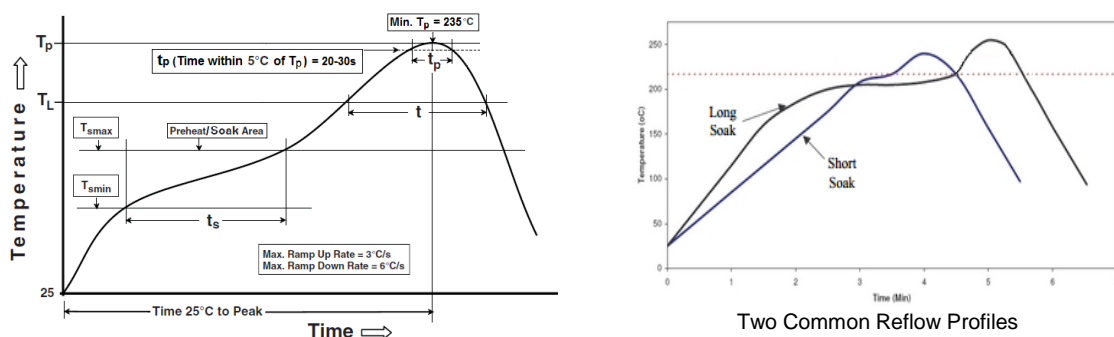
Good machine programming, process optimization and control are needed:

- Placement nozzle shape and drive is critical to regulate and control placing down the package without damage to the component thin structure, and adequate tack to paste to avoid component floating, paste displacement (squeeze out) or splatter.
- The Z-height optimally should be set at one-half the printed solder paste height.
- Board flatness is critical to maintain Z-height control.
- Machine with placement force control can be set between 1.5-3N, equipment type dependent.
- Misaligned parts <50% off the pad center can self-align during reflow. Self-alignment can be improved by using reflow in N2.

## Reflow Profile

Amkor DRMLF packages are lead-free. Refer to the package MSL specification for maximum allowed reflow temperature.

- Refer the solder paste supplier recommendation and guidelines of IPC-7093 and J-STD-020 in developing the optimum lead-free reflow profile.
- Recommend reflow peak temperature below the package max. MSL specification, to avoid unnecessary stress and/or damage to the package.
- Excessive soak, time above liquidus and peak temperatures can, in addition to causing more warpage of the package and PCB, deplete flux and cause re-oxidation of the solderable surfaces which may result in larger solder voids, splatter, brittle solder joints and poor wetting.
- The two most common profiles shown below (Figure 10) are influenced by oven efficiency, flux type, board size/mass and other components on the board.
  1. JEDEC guideline is a ramp-soak-spike (RSS) profile with a longer soak that equalizes temperatures across the higher density PCB and assemblies.
  2. Ramp-to-Spike/Peak (RTS) profile includes shorter linear ramp to peak temperature that is typically a good starting point for most common applications.



Reflow Profile	T <sub>Smin</sub>	T <sub>Smax</sub>	t <sub>s</sub>	T <sub>L</sub>	T (time above T <sub>L</sub> )	Max T <sub>p</sub>	Time to T <sub>p</sub>
JEDEC (long)	150°C	200°C	60-120 s	217°C	60-150 s	260°C	8 minutes max.
RTS (short)	150°C	180°C	30-60 s	217°C	45-75 s	245°C	4-6 minutes

Figure 10. Reflow Profiles for Lead-free SAC Solder Paste

## Inspection

DRMLF® exposed lead end/flank may not be fully solderable and a complete solder fillet formation on the side of the package after reflow soldering cannot be guaranteed.

- Visual optical inspection should be performed in accordance with IPC/EIA J-STD -001 and IPC A-610 as a “Bottom Only Termination”.
- Packages with wettable lead end/flank and extended board pad outside of package are inspectable for presence of periphery solder fillet with Automatic Optical Inspection (AOI).
- To inspect for open or short (bridging) and solder voids after reflow soldering, x-ray inspection is needed.
- Void limits in lead and thermal pad solder is by user application and/or agreement per J-STD/IPC, but thermal pad void <50% and lead void <25% are commonly acceptable.

## Rework

Rework-ability of DRMLF is highly dependent on complexity of the board design (layout and density). Therefore, the following only provides a guideline and a starting point for the development of a successful rework process for these packages.

- Retouch/touch up is limited to the outer row side fillet.
- To repair defects underneath the package, it must be removed.
- The removal and replacement process involves the following steps. Refer to guidelines J-STD-033 for handling of moisture sensitive devices and IPC-7711/7721 for rework and repair of bottom terminated component (BTC).
  - 1) Prebaking PCB and Package
    - a. Board and package must be free of moisture that can damage the assembly – prior to rework prebake at 125°C for 4-9 hours.
  - 2) Equipment and Tooling Set-up
    - a. A rework/repair system equipped with split-beam optical alignment capability  $\leq 0.5$  mm pitch, controlled top/bottom heating and auto vacuum pick/lift is needed. A system with focused infrared (IR) heater is an alternative (over traditional hot-gas) for accurate removal and replacement of the package without heating the tightly placed adjacent components.
    - b. Develop a reflow profile to heat DRMLF® including center pad solder joint to  $\sim 240^{\circ}\text{C}$ - $250^{\circ}\text{C}$  for  $\leq 90$  seconds with bottom side (board) preheated at  $\sim 180^{\circ}\text{C}$ - $200^{\circ}\text{C}$ , for lead-free process.
  - 3) Component Removal
    - a. Reflow the package solder
    - b. Vacuum lift/remove the package
  - 4) Site Redress/Preparation
    - a. PCB pads must be clean and level, wipe the land pad free of residual solder and flux.
  - 5) Solder Paste Application
    - a. Screen solder paste, using a mini stencil tool either onto the new DRMLF pads or onto the board land pads – paste, stencil thickness and aperture should be same as board mount process.
  - 6) Component Placement
    - a. Carefully align, place and reflow the new package.
  - 7) Inspection
    - a. Visually inspect periphery solder joints with 50-100X magnification.
    - b. X-ray package underside joints for open/short and excessive void.

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## Revision History

Rev	Description	Originator	Date
A	First release	DFOST	August 2005
B	Updated entire application note Updated land pad recommendation including additional packages Updated template Added company disclaimer	BZARK	August 2018
B1	Updated figures 1 and 4 image	BZARK	October 2018