Stacked CSP (SCSP)

The Stacked CSP family leverages Amkor's industry-leading ChipArray® Ball Grid Array (CABGA) manufacturing capabilities. This broad, high-volume infrastructure enables the rapid deployment of advances in die stacking technology across multiple products and factories to achieve lowest total cost requirements.

Stacked CSP technology enables the stacking of a wide range of different semiconductor devices to deliver the high level of silicon integration and area efficiency required in portable multi-media products.

Stacked CSP utilizes high-density thin core substrates, advanced materials (i.e., thin film die attach adhesive, fine filler epoxy mold compound), along with leading-edge wafer thinning, die attach, wirebonding and molding capabilities to stack multiple devices in a conventional fine pitch BGA (FBGA) surface mount component. These advanced assembly capabilities in combination with Amkor's expertise in design and test, enable stacks up to 16 active devices while optimizing yield and mounted height requirements.

Customers have relied on Amkor to solve their most complex and highest density device stack combinations. As a result, Amkor has established industry leadership in stacking pure memory, mixed signal and logic + memory devices, including NAND, NOR and DRAM memory, digital base band or applications processors + high density flash or mobile DRAM devices. Designers are looking to Stacked CSP technologies to achieve a high level of integration, along with size and cost reductions in future chip set combinations.

FEATURES

- 2-21 mm body size
- Package height down to 0.5 mm
- High die count pure memory, eMMC, eMCP and MCP
- Design, assembly and test capabilities that enable stacking of DRAM with logic or flash memory devices
- Logic/Flash, digital/analog and other ASIC/memory combinations of 320 I/O and greater
- Established package infrastructure with standard CABGA footprints
- Consistent product performance, high yields and reliability
- JEDEC standard outlines including MO-192 and MO-219
- Thin DA film and spacer technology, FoW and FoD
- Extended die overhang wirebonding
- Low loop wirebonding less than 35 µm
- Vacuum transfer and compression molding
- Wafer thinning/handling to 25 µm
- Pb-free, RoHS compliant and green materials
- Passive component integration options

Applications

SCSP is the best solution to address a range of design requirements, including:

- Higher memory capacity and more efficient memory architectures
- Smaller, lighter and more innovative product form factors
- Lower cost and more space efficiency

Reliability Qualification

Package Level

- Moisture sensitivity characterization: JEDEC level 3 @ 260°C; additional test data at: [(30°C/85% RH, 96 hours)+260] x2 or 3
- HAST: 130°C/85% RH, 96 hours
- Temp/Humidity: 85°C/85% RH, 1000 hours
- Temp cycle: -55°C/+125°C, 1000 cycles
- High temp storage: 150°C, 1000 hours

Board Level

- Thermal cycle: -40°C/+125°C, 1000 cycles

Amkor Technology®

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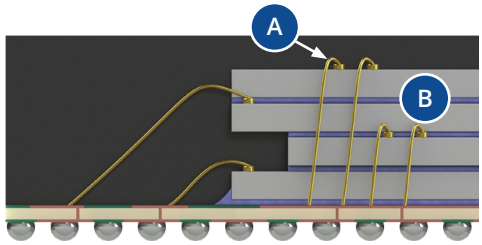
Process Highlights

- Die quantity, stack: Up to 24 high die configurations
- Ball pad pitch: 0.3, 0.4, 0.5, 0.65, 0.75, 0.8 mm
- Die thickness (min): Down to 25 µm
- Laminate core thickness: 40, 50, 60, 100 or 150 µm
- Ball diameter: 0.25, 0.30, 0.40, 0.46 mm
- Die bond pitch (min): 35 µm (in-line) with roadmap to 25 µm
- Wirebond length (max): 5 mm (200 mils)
- Wirebond diameter (min): 15, 18, 20, 25, 30 µm
- Low loop wirebonding: 35 µm
- Wafer thinning: 200 & 300 mm wafers

Standard Materials

- Package substrate
  - Dielectric: Laminate (e.g., DS7409, E679, BT polyimide (e.g., Kapton)
  - Layer count (laminate): 2-6
- Die attach: Film DA compatible with all passivation types
- Wire type: Ag, Gold, Cu, PCC, high tensile strength
- Encapsulant: Thixotropic epoxy (black)
- Solder balls: 63 Sn/37 Pb & Pb-Free Sn/3-4 Ag/0.5 Cu
- Device type: Silicon, SiGe, etc.
- Marking: Laser

Stacked CSP Key Technologies

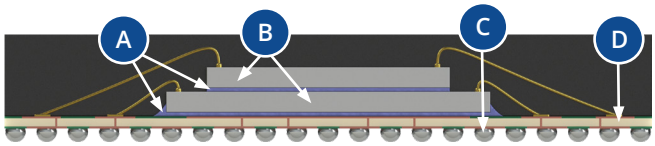


A Low loop wirebonding

B Film on wire

Stacked CSP Cross Section

2 Die On 2-Layer Laminate Structure



A Die attach film/paste

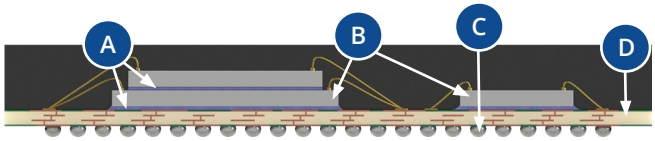
B Top and bottom die

C Solder ball

D Dielectric

Stacked CSP Cross Section

2 + 1 Die On 4-Layer Laminate Structure



A Die attach film/paste

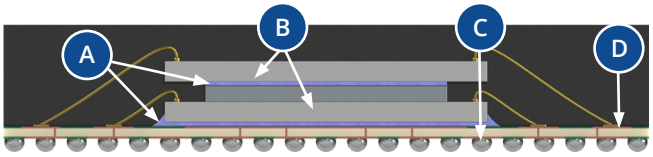
B Bottom and side die

C Solder ball

D Dielectric

Same Size (SS) Die Stacked CSP Cross Section

2 Die On 2-Layer Laminate Structure



A Die attach film/paste

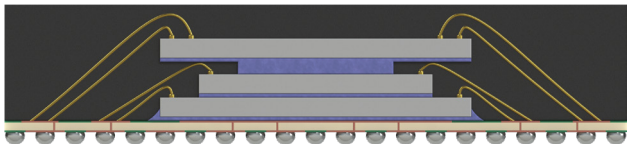
B Top and bottom die

C Solderball

D Dielectric

Stacked CSP Cross Section

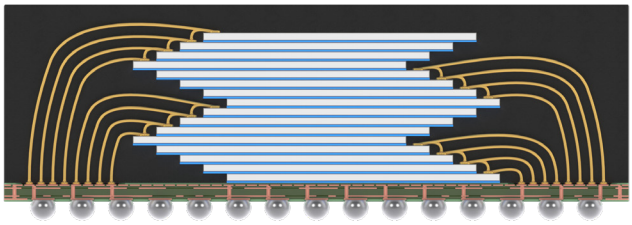
3 + 1 Logic + Memory



Stacked CSP (SCSP)

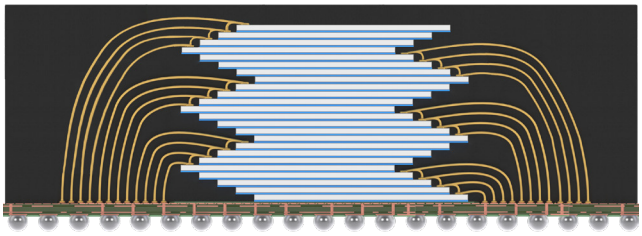
Stacked CSP Cross Section

16 + 0 Die Memory



Stacked CSP Cross Section

24 + 0 Die 3D Memory



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