SWIFT® Technology

Silicon Wafer Integrated Fan-out Technology (SWIFT) is designed to provide increased I/O and circuit density in a reduced footprint and profile for single and multi-die applications. SWIFT technology enables creation of advanced 3D structures, addressing the need for increased IC integration in emerging mobile and networking applications.

SWIFT® PACKAGING CONSIDERATIONS

Amkor's state-of-the-art High-Density Fan-Out (HDFO) structure called Silicon Wafer Integrated Fan-out Technology (SWIFT) packaging, bridges the gap between TSV and laminate substrates.

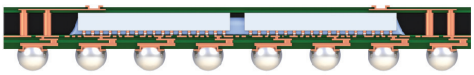
FEATURES

- Polymer dielectrics
- Multi-die and large die capability
- Large body package capability
- Interconnect density down to 2/2 µm
- Cu pillar die interconnect down to 30 µm pitch
- Meets JEDEC MSL2a and MSL3 CLR and BLR requirements

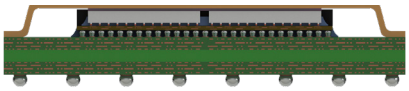
The distinctive characteristics of SWIFT technology are due, in part, to the fine feature capabilities associated with this innovative wafer level packaging technique. This allows more aggressive design rules to be applied compared to traditional WLFO and laminate-based assemblies.

SWIFT Structures and Attributes

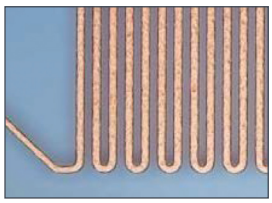
The figure below shows cross-section illustrations of a single die SWIFT and dual-die 3D/Package-on-Package (PoP) SWIFT structures. Although the package appears to be of a typical fine-pitch flip chip construction, it incorporates some unique features not associated with conventional IC packages.



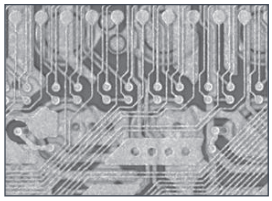
Fan-in PoP SWIFT®



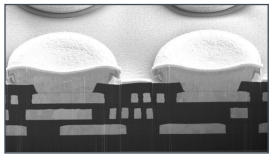
SWIFT® on Substrate



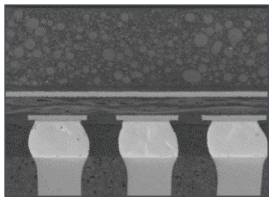
Plated Cu RDL L/S down to 2 µm



Multilayer Redistribution



Multilayer RDL Cross Section



Tall Cu Pillar for PoP Applications

Enabling Technologies for SWIFT Packaging

Key assembly technologies enable the creation of these distinctive SWIFT packaging features and attributes. Through the use of stepper photo imaging equipment, 2/2 µm line/space features can be achieved, enabling very high density die-to-die connections required for SoC partitioning and networking applications where 2.5D TSV would typically be used. Fine-pitch die micro bumps provide a high-density interconnect for advanced products, such as application processors and baseband devices. In addition, tall Cu pillars enable a high-density vertical interface for mounting advanced memory devices on the top of the SWIFT structure.

Amkor Technology®

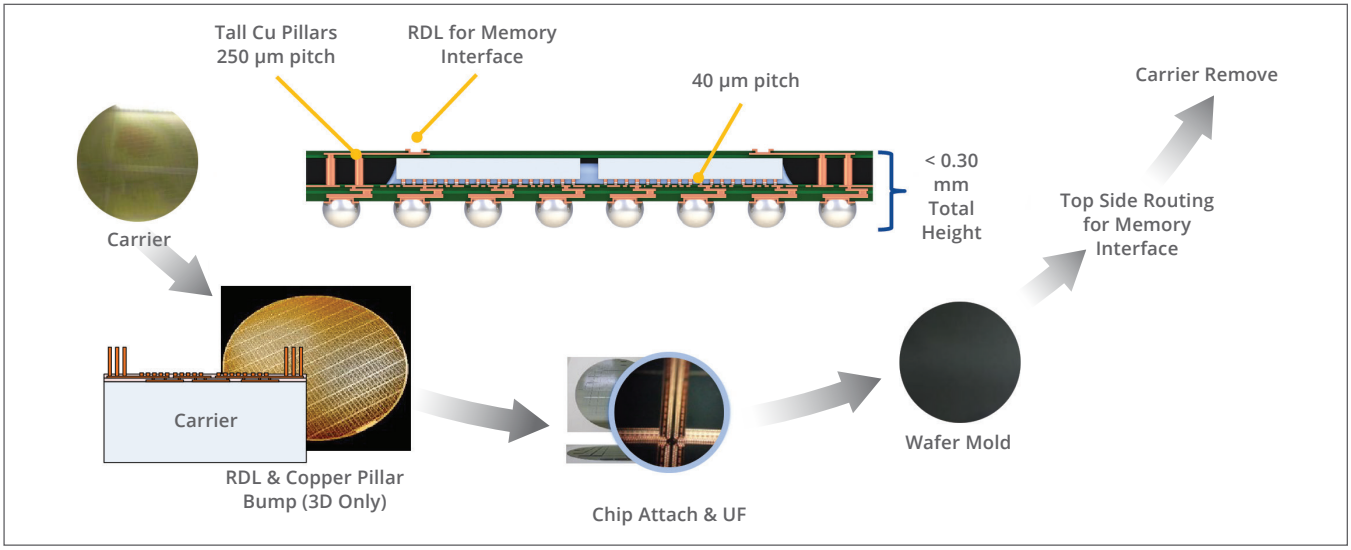
SWIFT® Technology

SWIFT Packaging Process Flow

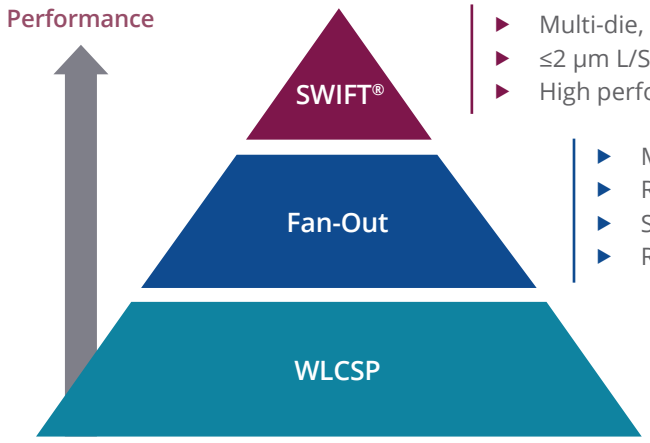
SWIFT product attributes are realized by applying a unique process flow that incorporates both flip chip assembly and wafer level processing techniques, as shown below.

Reliability Data					
Component Level				Board Level	
MSL2aA, MSLA3 Precon	Unbiased HAST 192 hrs	TCB 1500 cycles	HTS 1000 hrs	Drop	Temp Cycle
Pass	Pass	Pass	Pass	Pass	Pass

SWIFT Packaging Technology Process Flow



Advanced Wafer Product Positioning



- Multi-die, SoC partition, 3D PoP-compatible
- ≤2 µm L/S routing by foundry BEOL interposer
- High performance (CPU/GPU), mobile AP, BB

- Multi-die, SoC partition, HBM, 3D PoP-compatible
- RDL 2~10 µm by Amkor bump line; mobile AP/BB
- Single or multi-die integration
- RDL 6~12 µm by Amkor bump line; RFIC & PMIC

- Single die
- RDL ≥10 µm by Amkor bump line
- RF, WLAN, Power, etc.

Products: RF and analog to advanced processors

Visit amkor.com or email sales@amkor.com for more information.