Package-on-Package (PoP)

BENEFITS AS AN ENABLING TECHNOLOGY

PoP offers OEMs and EMS providers a flexible platform to cost effectively integrate logic plus memory devices in a 3D stacked architecture. Integration through PoP provides technical and business/logistics benefits.

- Greatly expands device and supplier options by simplifying the business logistics of stacking
- Integration controlled at the system level to best match stacked combinations including memory architecture with the system requirements
- JEDEC standards ensure broad component availability
- Improving time-to-market, inventory management and supply chain flexibility
- Eliminates margin stacking and expands technology reuse
- Provides the lowest total cost of ownership where complex 3D integration of logic plus memory is required

Bottom PoP Technologies

Amkor's popular Package Stackable Very Thin Fine Pitch BGA (PSvfBGA) platform supports single die, stacked die using wirebond or hybrid (FC plus wirebond) stacks and has been applied to Flip Chip (FC) applications to improve warpage control and package integrity through test and SMT handling.

As handheld microprocessors have transitioned to advanced CMOS nodes with higher speed cores with higher I/O, there has been a transition from wirebond to flip chip die designs. Flip chip enables the use of an exposed die bottom package that integrates the package stacking design features of PSvfBGA in a fcCSP assembly flow, which Amkor calls Package Stackable Flip Chip Chip Scale Package (PSfcCSP). PSfcCSP has a thin exposed FC die enabling fine pitch stacked interfaces at 0.5 mm pitch which is a challenge in a center molded PSvfBGA structure.

Continued development resulted in Amkor entering the second generation of PoP applications where new memory architectures, required in mobile multimedia applications, demand higher density stacked interfaces in combination with PoP mounted area and height reductions. The previous PSvfBGA and PSfcCSP structures limited the ability of the memory interface to scale in density and pitch, resulting in the need for a new bottom PoP structure.

Amkor developed new technologies to create the next-generation PoP solution with interconnect vias through the mold cap. Known as Through Mold Via (TMV®), this technology provides a stable bottom package that enables use of thinner substrates with a larger die to package ratio. TMV® enabled PoP can support single, stacked die or FC designs. TMV® is an ideal solution for the emerging 0.4 mm pitch low power DDR2 memory interface requirements and enables the stacked interface to scale with solder ball pitch densities to 0.3 mm pitch or below.

The next few years promise to provide many new challenges and applications for PoP, as handheld multimedia applications continue to demand higher signal processing power and data storage capabilities. Amkor is committed to maintaining strong development and production capabilities to ensure we are at the forefront in meeting next-generation PoP requirements.

Applications

PoP packages are designed for products requiring efficient memory architectures including multiple buses and increased memory density and performance, while reducing mounted area. Portable electronic products such as mobile phones (baseband or applications processor plus combo memory), digital cameras (image processor plus memory), portable media players (audio/graphics processor plus memory), gaming and other mobile applications can benefit from the combination of stacked package and small footprint offered by Amkor's PoP family.

Amkor Technology®

Features

- 10-15 mm body sizes tooled per product table, additional sizes based on demand
- Top package I/O interface 0.65 mm pitch accommodating 104 to 160 pin counts
- Wafer thinning/handling <100 µm
- Mature PoP platform with consistent product performance and reliability
- Package configurations compliant with JEDEC standards
- Bottom PSvfBGA and top FBGA/Stacked CSP packages are well established in high volume production with multi-region and factory support
- Stacked package heights of 1.3 mm to 1.5 mm available in a variety of configurations (See Stack Up Tables on following pages)

Process Highlights

- Die thickness: 75 µm to 125 µm
- Bond pad pitch (min): 45 µm (in-line)
- Marking: Laser
- Wafer thinning: 200 & 300 mm wafers

Test Services

- Program generation/conversion
- Product engineering
- Dual sided contactor system available
- Tape and reel services

Standard Materials

- Standard RoHS and green material sets available
- Package substrate
  - Conductor: Copper
  - Dielectric: Thin core FR5 or equivalent
- Die attach adhesive: Conductive or non-conductive
- Encapsulant: Epoxy mold compound
- Solder ball: Pb-free

Reliability Qualification

Amkor assures reliable performance by continuously monitoring key indices.

Package Level

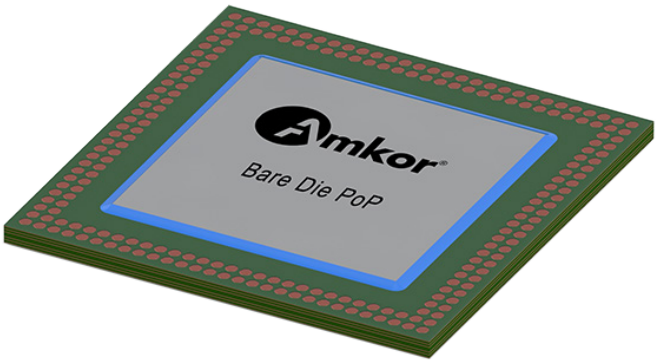
- Moisture resistance testing: JEDEC level 3 @ 260°C x 3 reflows
- Additional test data: 30°C, 85% RH, 96 hours @ 260°C x 4
- uHAST: 130°C, 85% RH, 96 hours
- Temp/Humidity: 85°C, 85% RH, 1000 hours
- Temp cycle: -55°C/+125°C, 1000 cycles
- High temp storage: 150°C, 1000 hours

Board Level

- Thermal cycle: -40°C/+125°C, 1000 cycles

Package Dimensions

- PSvfBGA: 10 x 10 mm to 15 x 15 mm
- PSfcCSP: 12 x 12 mm to 13 x 13 mm
- TMV® PoP: 12 x 12 mm to 14 x 14 mm



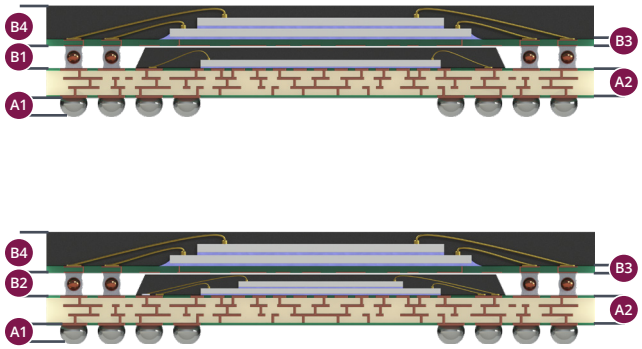
Shipping

- JEDEC trays

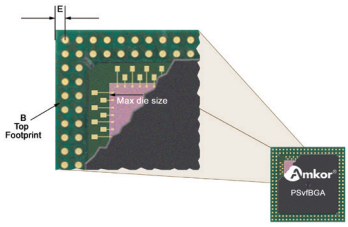
Cross Section PoP

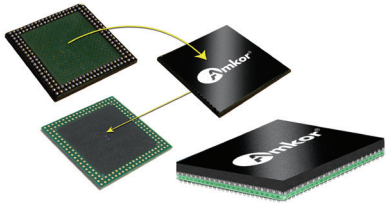
PoP Overall Stack Up Table (mm)

Symbol	FBGA + PSvfBGA		
	Min	Max	Nom
A1 (Mounted, 0.5 Pitch)	0.180	0.280	0.230
A2 (4L Laminate)	0.260	0.340	0.300
B1 (Stacked, 0.65 Pitch), Single Die	0.270	0.330	0.300
B2 (Stacked, 0.65 Pitch), 2+0 Die	0.320	0.380	0.350
B3 (2L Laminate)	0.100	0.160	0.130
B4 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.300	1.500	1.400



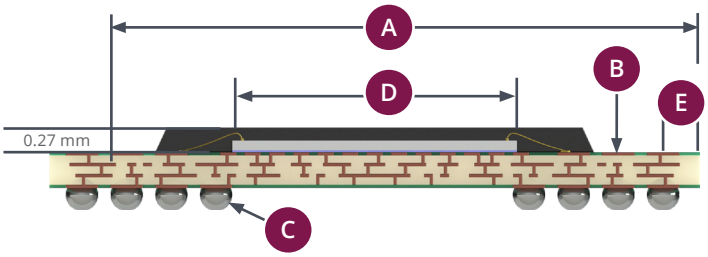
PSvfBGA Top View





Stacked Package

Cross Section PSvfBGA



- A Package size
- B Top footprint
- C Bottom footprint
- D Max die size

PSvfBGA Design Table For 0.65 mm Pitch 2 Row Stacked Interfaces

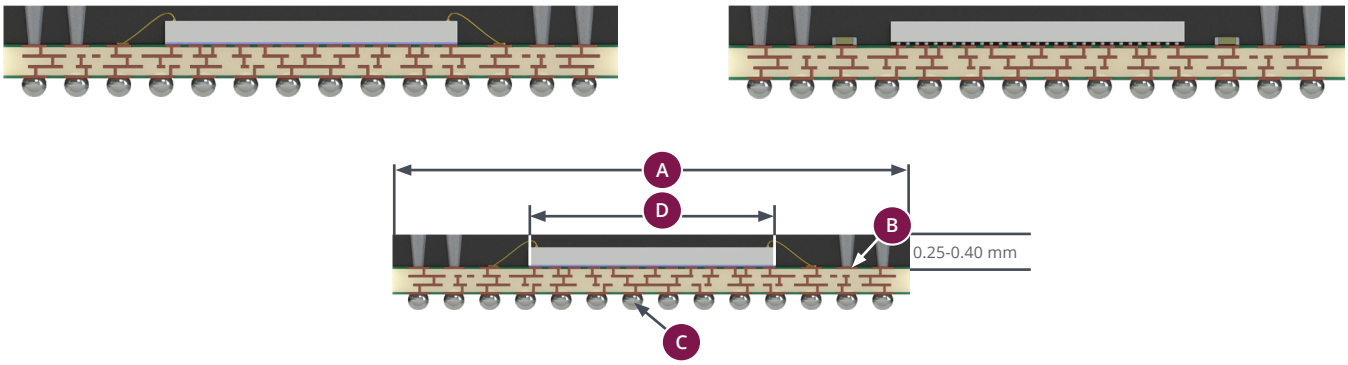
A	B		C	D	E	Typical Wirecount For Given Package Size
Body Size (mm)	Package Interconnect		Bottom Package Ball Count Nom	Die Size (mm)	Package Interconnect Ball Center To Package Edge (mm)	
	Matrix	Ball Count				
10	15	104	300	< 5.50	0.450	320
11	16	112	350	< 6.00	0.625	360
12	18	128	400	< 7.50	0.475	420
13	19	136	450	< 8.00	0.650	460
14	21	152	550	< 9.00	0.500	520
15	22	160	650	< 10.00	0.675	600

Dimensions are in line with JEDEC JC-11 standards for PoP packages in development

B - Based on 2 perimeter rows of interconnects at 0.65 mm pitch

C - Based on 4 perimeter rows of BGA balls to motherboard at 0.50 mm pitch

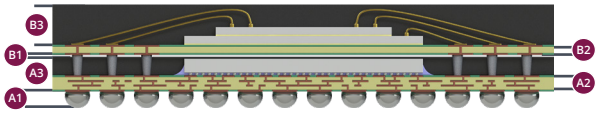
Cross Section TMV® PoP



TMV® Design Table For 0.4 mm Pitch 2 Row Stacked Interfaces

A	B		C	D	E
Body Size (mm)	Package Interconnect - 2 Rows		Bottom Package 0.4 mm Pitch (Full Matrix)	Max Die Size Flip Chip (mm)	Package Interconnect Ball Center To Package Edge (mm)
	Matrix	Top Ball Count			
10	23	168	529	7.00	6.00
11	26	192	676	8.00	7.00
12	18	128	400	< 7.50	0.475
13	19	136	450	< 8.00	0.650

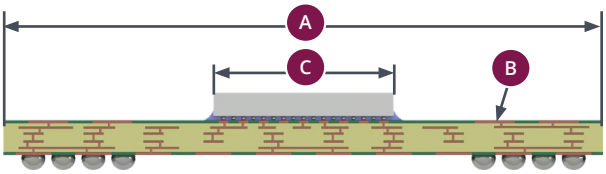
Cross Section TMV® PoP



TMV® Overall Stack Up Table (mm)

Symbol	Min	Max	Nom
A1 (Mounted, 0.4 pitch)	0.100	0.200	0.150
A2 (4L Laminate)	0.220	0.300	0.260
A3 (Mold Cap)	0.230	0.280	0.250
B1 (Stacked Gap)	0.020	0.080	0.050
B2 (2L Laminate)	0.100	0.160	0.130
B3 (Mold Cap)	0.370	0.430	0.400
Overall Package Height	1.140	1.340	1.240

Cross Section PSfcCSP



PSfcCSP Design Table For 0.5 mm Pitch 2 Row Stacked Interfaces

A	B		C
Body Size (mm)	Package Interconnect		Die Size (mm)
	Matrix	Ball Count	
10	19	136	< 6.00
11	21	152	< 7.00
12	23	168	< 8.00
13	25	184	< 9.00
14	27	200	< 9.50
15	29	216	< 10.00

Visit amkor.com or email sales@amkor.com for more information.