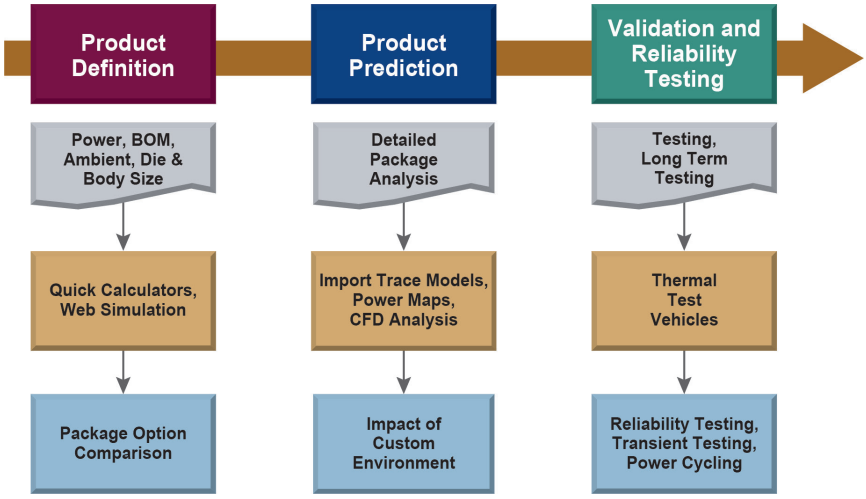
# Mechanical Package Characterization

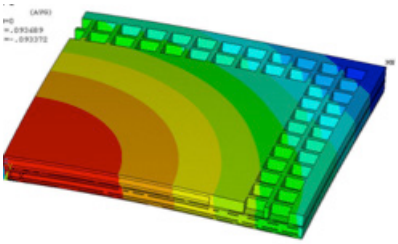
Mechanical package characterization is an integral part of Amkor's product development and characterization. During product definition stage, quick calculators and numerical Design of Experiments (DOEs) are used to select design attributes and materials meeting performance and reliability requirements. A more detailed set of simulations are then performed on actual designs incorporating substrate and die details. Finally, simulation results are validated with actual warpage measurements and reliability testing on engineering samples.

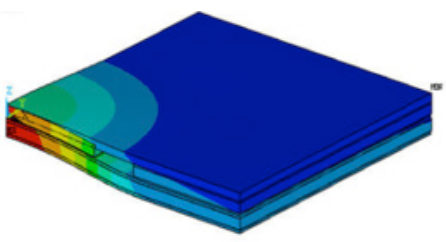



## Package Warpage

- One of the key considerations for IC packages, especially thin 3D and PoP packages
- Warpage is caused by the CTE mismatch of various materials involved and is typically temperature dependent
- Excessive warpage can cause shorts, non-wets or de-wets during the board assembly process

Amkor offers package warpage prediction using a finite element method for all package types. Warpage predictions are provided for both room and elevated temperatures to help optimize package design and material parameters.





## MECHANICAL TESTING AND CHARACTERIZATION OFFERINGS

- Temperature-dependent property measurement (modulus, CTE, Tg by DMA/TMA)
- Nano-indentation (extract property of thin layers)
- Solder joint creep property measurements
- Mechanical strength testing (load vs displacement)
- Electromigration as function of temperature, time current and interconnect
- Bump shear
- Failure analysis using optical inspection, event detection, resistance increase
- Warpage measurement at room temperature and under reflow conditions
- Reliability testing; thermal cycling, high temperature storage and humidity
- Power cycling and in-situ interconnect monitoring
- Drop testing
- Three/four-point bend testing
- Surface mount assembly support

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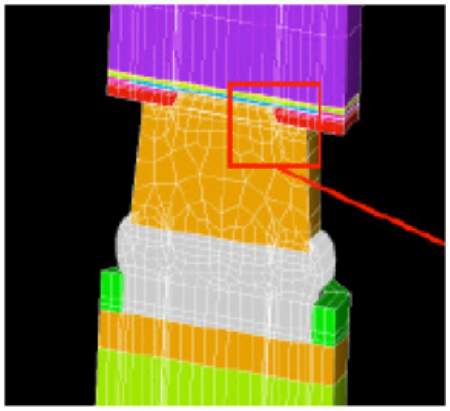
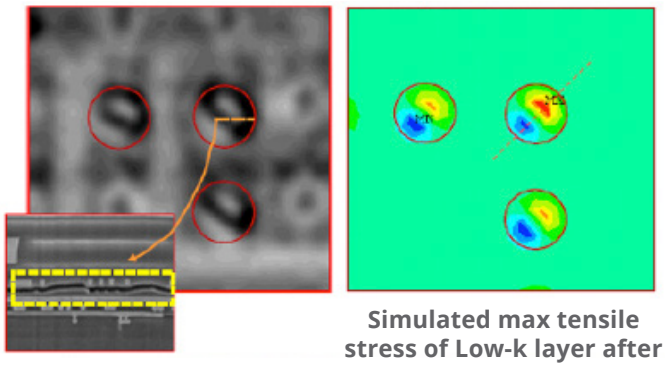
## Interconnects And Die/Low-k Stress

- Prediction of stress due to reliability testing or from assembly processes
- Stress prediction at different interfaces or bulk materials such as die, ELK, UBM, Cu pillar, solder bump, substrate Cu trace
- Correlation of stress levels to various failure modes and locations to avoid potential reliability concerns



**White bump by SAT (Low-k damage) at die corner**

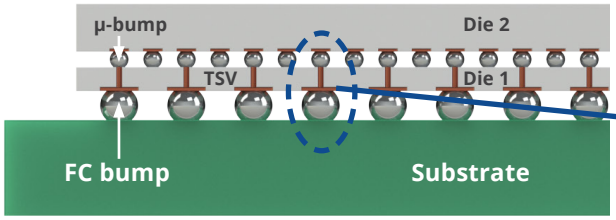


**Simulated max tensile stress of Low-k layer after chip attach at die corner**

## Chip Package Interaction

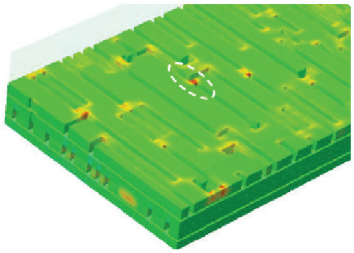
- Advanced chip/Low-k design performance can be affected by the external stress/strain load generated from the package
- Amkor is capable of setting up the package level mechanical model and provides the specified boundary loading results to customers for their in-house Si/Low-k level model/design tool. This helps in optimizing design up front and facilitates chip-package co-design

**Amkor's package level model**

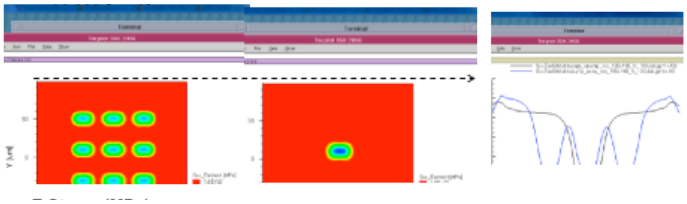



**Boundary output transfer**

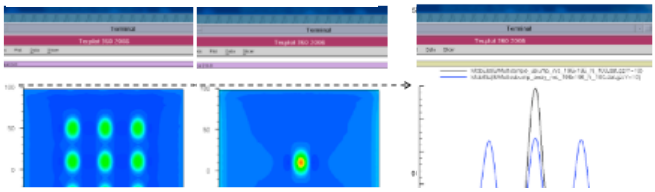
**Customer's Si/Low-k level model**



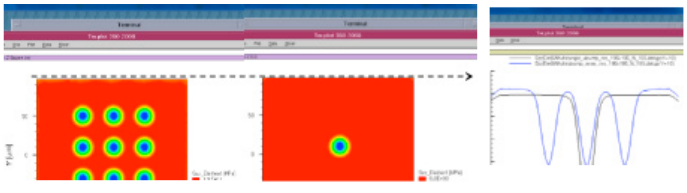
**X-Stress (MPa)**



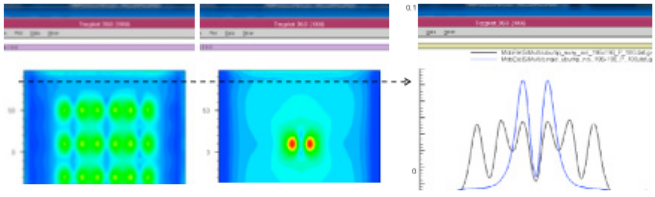
**Mobility change: NMOS**



**Z-Stress (MPa)**



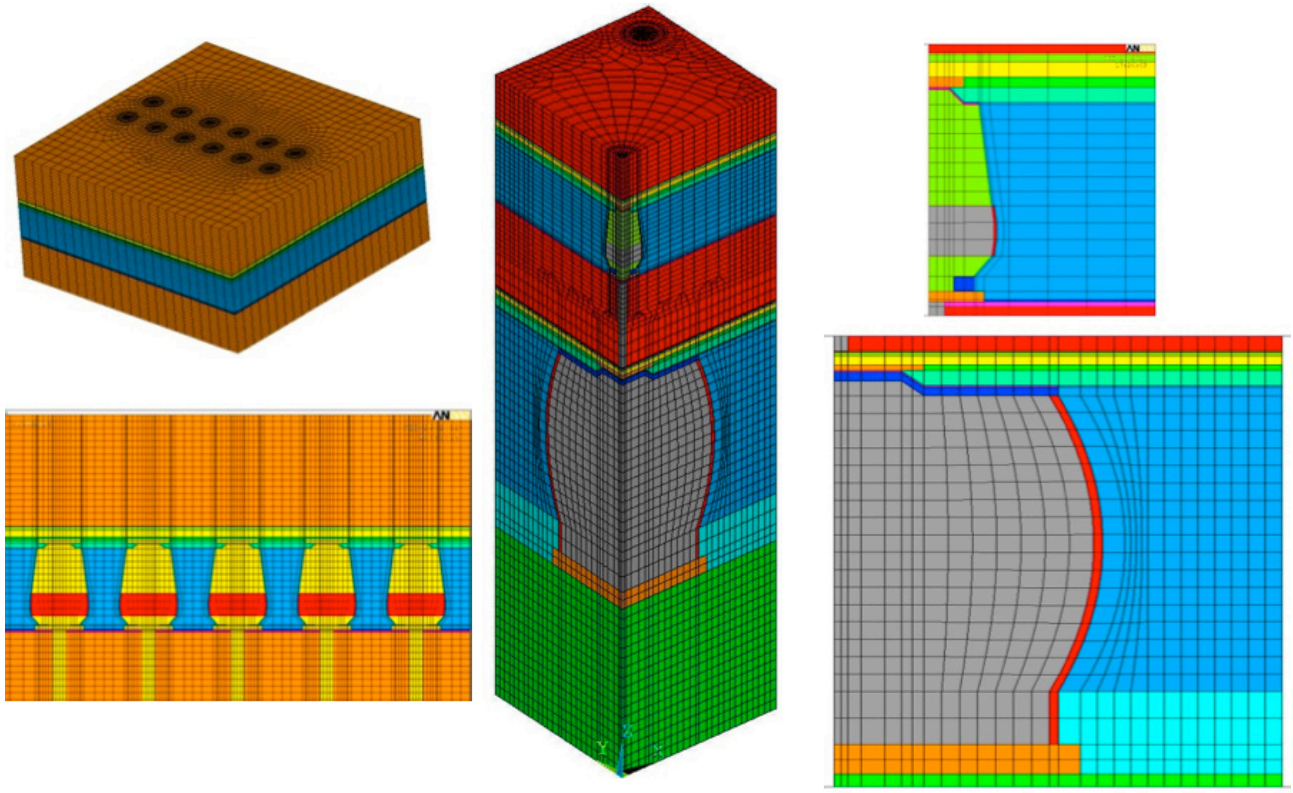
**Mobility change: PMOS**



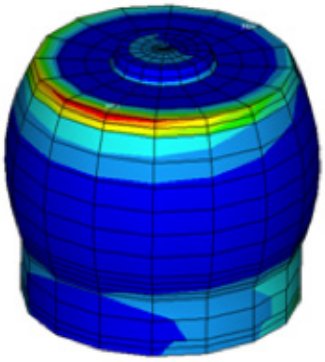
# Mechanical Package Characterization

## 3D Package Model

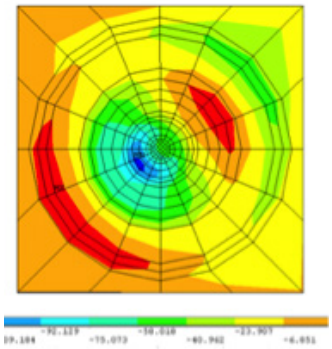
- For Through Silicon Via (TSV), Package-on-Package (PoP), Through Mold Via (TMV®), Wafer Level Package (WLP) and System in Package (SiP)
- Simulations for design and material impact on stress at TSV, µ-bump, flip chip bump, RDL layer for potential failure as well as warpage prediction for 3D IC and 3D package configurations



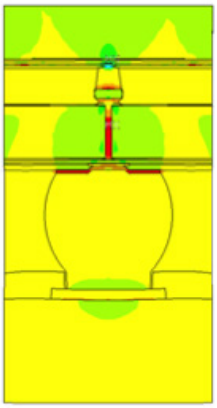
**Bump stress**



**Low-k stress**

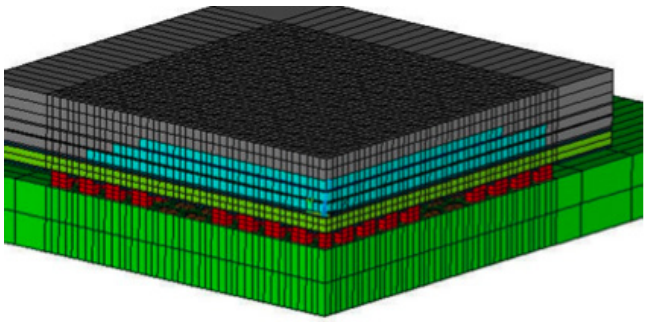


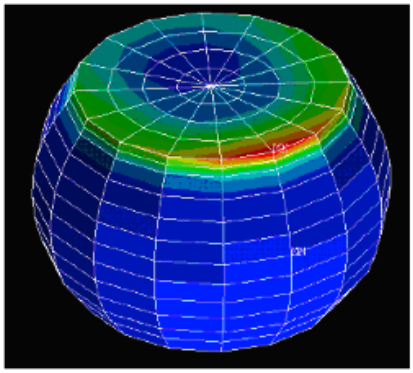
**TSV stress**

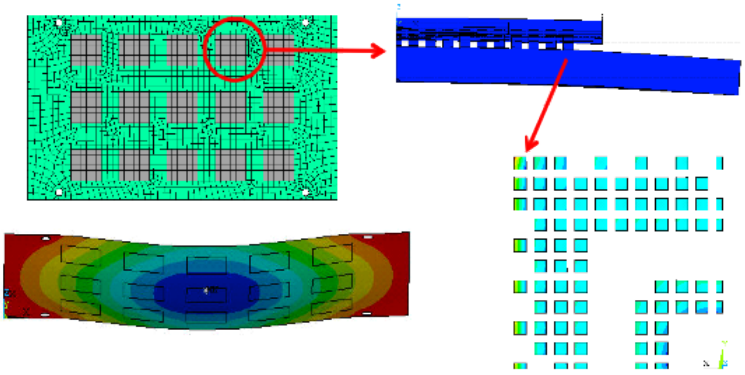


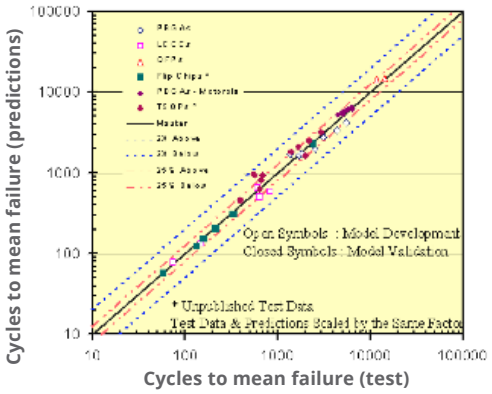
## Board Level Reliability (BLR) Prediction

- Solder joint life prediction for temperature and power cycling: finite element based simulation provides a quick estimation of expected reliability and is used extensively in the pre-design stage. The life prediction approach correctly predicts the location of critical solder joints and location of failure (board or package side) with a high degree of accuracy for actual values
- Board level drop test simulation: provides relative comparison for package material and design attributes



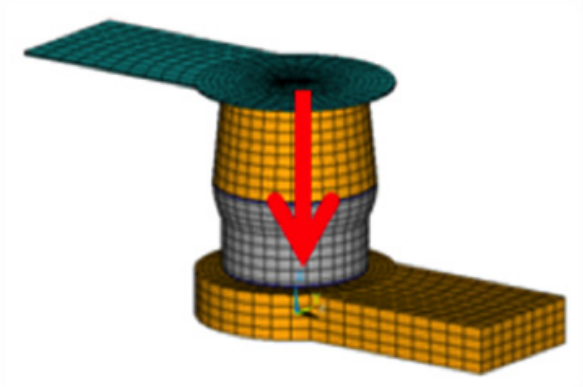


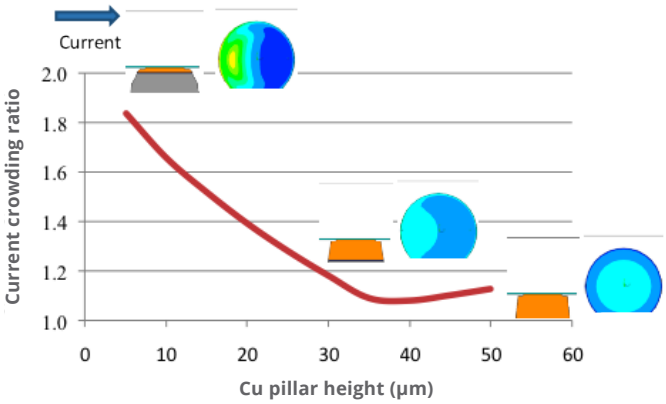





## Electromigration Model

- Provides estimation of current density distribution within an interconnect
- Simulations are used to determine the impact of bump design on current density distribution and potential electromigration reliability

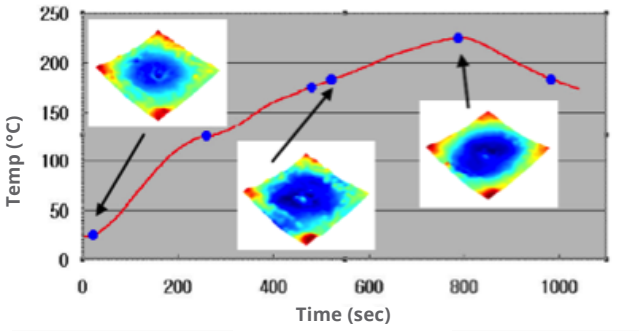




# Mechanical Package Characterization

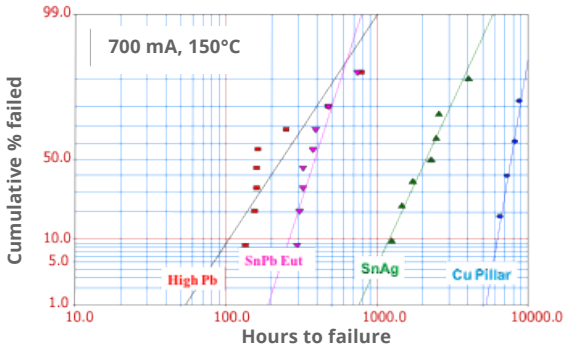
## Warpage Shadow Moire Measurement

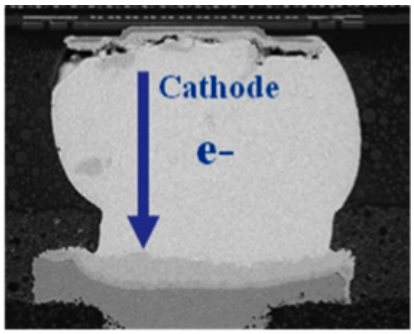
- Full compliance with JEDEC JESD22B112 standard
- Warpage at room and elevated temperatures




## Electromigration Test

- Test capability to test low and high-current applications
- Data collected on flip chip bumps, µ-bumps, Cu pillars and Wafer Level Chip Scale Packaging (WLCSP)




## Board Level Reliability

Board level reliability is one of most important aspects of package selection. Electronic assemblies experience varied field use stress conditions during their useful life and package-to-board interconnects are required to survive these conditions. As part of our strategy to provide complete packaging solutions to our customers, Amkor offers solder joint reliability characterization of all package styles.

## Temperature Cycle Tests

Amkor employs the following three temperature cycle test conditions for board level reliability, depending on the intended end use application of the package. All three of these conditions comply with IPC-9701 specifications. In-situ electrical testing is performed to identify failures.

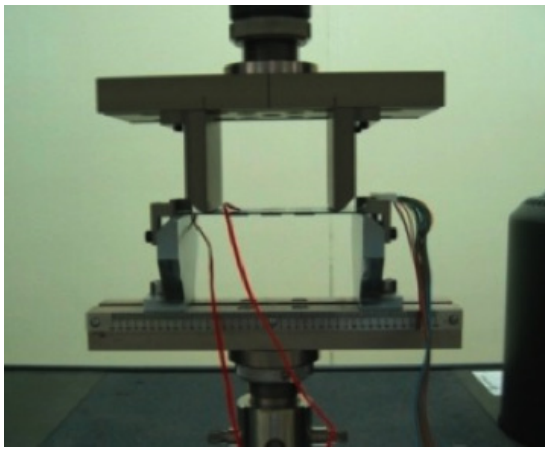
| Condition (°C) | Min Temp (°C) | Max Temp (Minutes) | Ramp Up Time (Minutes) | Ramp Down Time (Minutes) | High Temp Dwell (Minutes) | Low Temp Dwell (Minutes) | Cycle Duration (Minutes) |
|---|---|---|---|---|---|---|---|
| TC1 | -40 | 125 | 15 (+5/-0) | 15 (+5/-0) | 15 (+0/-5) | 15 (+0/-5) | 60 |
| TC2 | -55 | 125 | 2-3 | 2-3 | 12-13 | 12-13 | 30 |
| TC3 | 0 | 100 | 10 (+2/-0) | 10 (+2/-0) | 10 (+0/-2) | 10 (+0/-2) | 40 |

## Board Level Drop Tests

This test is implemented to provide a controlled environment to reproduce the interconnect failure mode commonly experienced during drop of handheld electronic systems (e.g., mobile phones, PDAs, etc.). The testing is conducted as per JEDEC standard (JESD22-B111). Amkor is also certified by Nokia and Motorola for testing according to their test methods.

## Cyclic Bend Test

The cyclic bend test consists of bending the printed circuit board assemblies using a 4-point bend test fixture. This test may be used to reproduce solder joint failures experienced in package mounted on key pads.



Visit amkor.com or email sales@amkor.com for more information.