

FlipStack® CSP



FEATURES

- ▶ Package height down to 0.6 mm
- ▶ Design, assembly and test capabilities that enable stacking combinations of memory, logic and mixed signal type devices
- ▶ Established package infrastructure with standard CABGA and fcCSP footprints
- ▶ Consistent product performance with high yields and reliability
- ▶ Die overhang wirebonding
- ▶ Low loop wirebonding to 40 µm or less
- ▶ Pb-free, RoHS compliant and green materials
- ▶ Passive component integration options
- ▶ JEDEC standard outlines including MO-192, MO-195, MO-216, MO-219 and MO-298

The FlipStack® CSP family utilizes Amkor's industry leading ChipArray® Ball Grid Array (CABGA) manufacturing capabilities, in combination with Amkor's fcCSP technology. This broad high-volume infrastructure enables the rapid deployment of advances in die stacking technology across multiple products and factories to achieve lowest total cost.

FlipStack® CSP technology enables the stacking of a wide range of different semiconductor devices to deliver the high level of silicon integration and area efficiency required in portable multi-media products. This type of packaging uses high density thin core substrates, advanced wafer thinning, die attach, flip chip and wire bonding capabilities to stack multiple devices in a conventional fine pitch BGA (FBGA) surface mount package.

Many customers have relied on Amkor to solve their highest density and most complex device stack combinations. As a result, Amkor has established industry leadership in stacking complex mixed signal, logic + memory devices, including digital base band or application/processors + high density flash or mobile DRAM devices. Designers are looking to FlipStack® CSP technologies to achieve integration, size and cost reductions in chip set combinations.

Applications

FlipStack® CSP technology enables smaller, lighter and more innovative new product form factors at a lower cost. This solution addresses a range of design requirements, and enables a wide variety of applications, including portable multimedia devices such as tablets, cell phones and digital cameras.

Reliability Qualification

Amkor assures reliable performance by continuously monitoring key indices.

- ▶ Moisture resistance testing: JEDEC level 3 @ 260°C
- ▶ Biased/Unbiased HAST: 121°C/100% RH, 2 atm, 192 hours
- ▶ Temp/Humidity: 85°C/85% RH, 1000 hours
- ▶ Temp cycle: -55°C/+125°C, 1000 cycles
- ▶ High temp storage: 150°C, 1000 hours

Board Level

- ▶ Thermal cycle: -40°C/+125°C, 1000 cycles

Test Services

- ▶ Program generation/conversion
- ▶ Product engineering
- ▶ Wafer sort
- ▶ -55°C to +165°C test available
- ▶ Burn-in capabilities
- ▶ Tape and reel services

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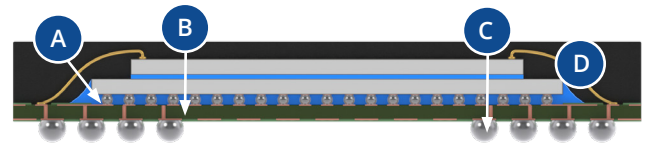
Standard Materials

- ▶ Package substrate
 - ▷ Laminate dielectric
 - » HL832: NXA, NS, NS-LC, NSF-LCA
 - » E679: FG, FGB, FGBS, GT, E700G, E705G, DS7409HG, DS7409HGB(S), DS7409HGB(LE), ELC4785GSB, ELC4785THB, ELC4785THG
 - ▷ Layer count (laminate): 2-6
- ▶ Die attach
 - ▷ Bottom die: Flip chip attached by mass reflow or thermal compression
 - ▷ Top die: Non-conductive epoxy, film
- ▶ Wire type: Au, Cu or Ag
- ▶ Encapsulant: Transfer molded epoxy
- ▶ Underfill: Capillary or molded
- ▶ Bumps (F/C die): Pb-free, eutectic, Cu pillar
- ▶ Solder balls: Pb-free, eutectic
- ▶ Device type: Silicon, SiGe, GaAs, glass (IPD film on glass)
- ▶ Marking: Laser

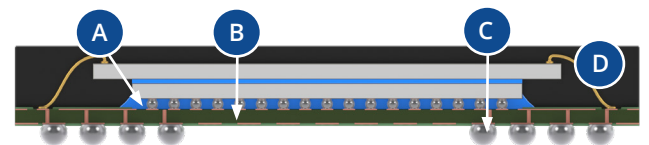
Process Highlights

- ▶ Ball pad pitch: 0.35, 0.4, 0.5, 0.65, 0.75, 0.8, 1.0 mm
- ▶ Die thickness (flip chip): As thin as 70 μm
- ▶ Die thickness (wirebond): As thin as 50 μm
- ▶ Ball diameter: As required
- ▶ Wirebond pitch (min): 40 μm in-line with roadmap to 25 μm
- ▶ Bump pitch mass reflow: 60 μm in-line
- ▶ Thermal compression: 50 μm in-line
- ▶ Wirebond length (max): 5 mm (200 mils)
- ▶ Wirebond diameter (min): 0.7, 0.8, 0.9, 1.0 mil+ in gold, silver or copper wirebond diameters
- ▶ Wafer diameter: 150, 200 & 300 mm wafers

Cross Sections



- A** Capillary or molded underfill options
- B** 2-6 Layer substrates
- C** Eutectic or lead-free solder ball options
- D** Gold, silver or copper wire options



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