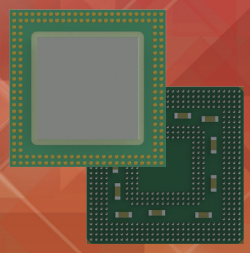
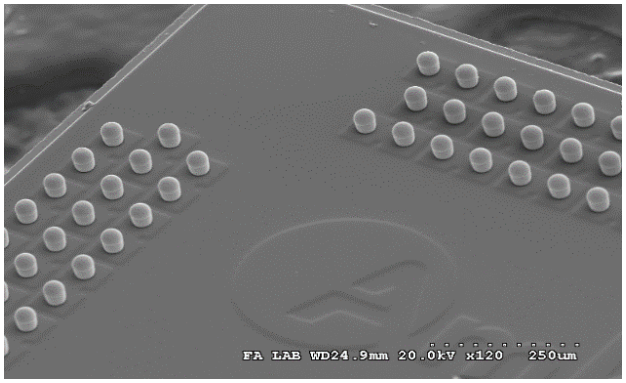
Copper Pillar

Copper pillar bump is widely used for many types of flip chip interconnect which offers advantages in many designs while meeting current and future ROHS requirements. It is an excellent interconnect choice for applications such as transceivers, embedded processors, application processors, power management, baseband, ASICs and SOCs where some combination of fine pitch, ROHS/Green compliance, low cost and electromigration performance are required.

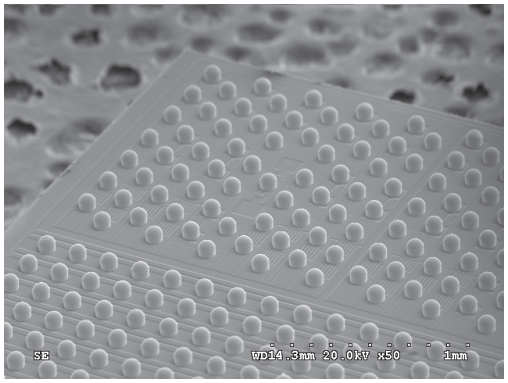


BENEFITS OF COPPER PILLAR

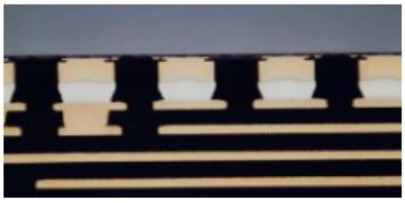
- Fine pitch capable down to 30 µm in-line and 30/60 µm staggered
- Cost reduction achievable in many designs by reducing substrate layer counts
- Superior electromigration performance for high-current carrying capacity applications
- Electrical test at wafer level prior to copper pillar bump
- Compatible with bond pad opening/pitch and pad metallization of die designed for wirebond which enables quick time-to-market for conversion to flip chip
- Lower cost fine pitch flip chip (FPFC) interconnect versus Au stud bump for high bump density designs
- Lead-free bump cap on copper pillar for green solutions
- Various Cu pillar structures available from Cu bar type, standard Cu pillar, fine pitch Cu pillar and micro-bumps. Also, available in different stack-ups from Cu+Ni+Pb-free, Cu+Ni+Cu +Pb-free depending upon application requirements
- Available with and without repassivation
- Qualified for advanced silicon node Low-k devices
- Small fillet requirement for underfill enables more aggressive die-to-package design rule/smaller package footprint
- Extreme fine pitch on silicon package down to 30 µm for TSV and CoC
- Large installed capacity for turnkey FPFC copper pillar bump, assembly and test

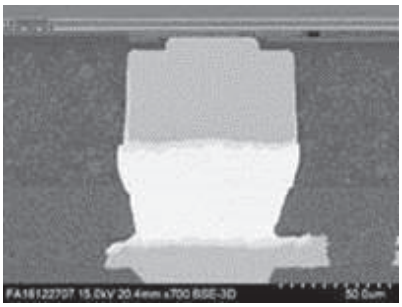


Peripheral Cu pillar bump



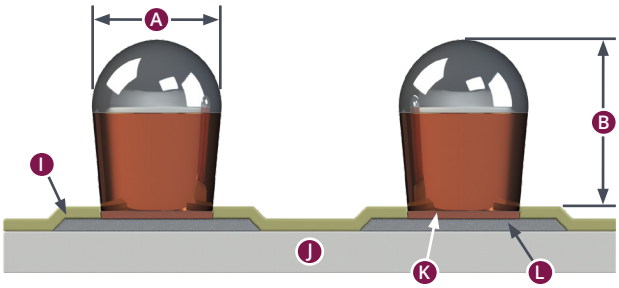
Full array Cu pillar bump



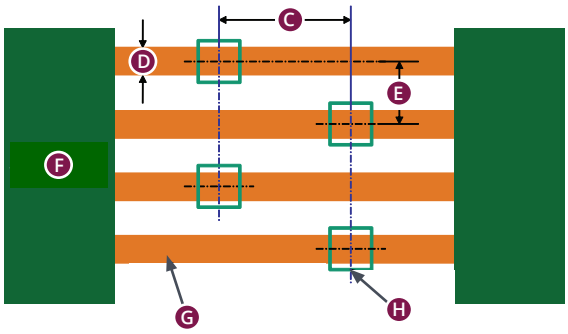


FCBGA chip to chip bonding with Cu pillar

Copper Pillar Bump Design Rules



	Feature	Dimensions
A	Cu Pillar Diameter	20-65 µm
B	Total Height	20-75 µm



	General Design Rules	Pitch				
		60	50	45/90	40/80	30/60
C	Row to Row Pitch	N/A	N/A	90	80	60
D	Bond Pad Width	30	25	22	20	TBD
E	Trace Pitch	60	50	45	40	30

F Solder mask

G Bond pad

H Die pad opening

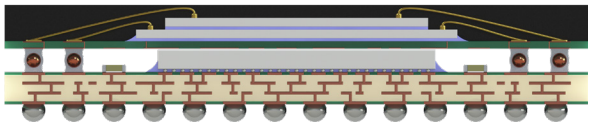
I Passivation

J Si Wafer

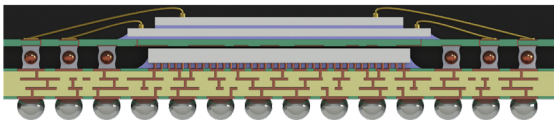
K UBM

L Al pad

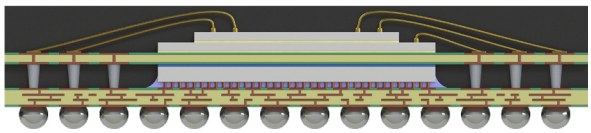
Cross Sections



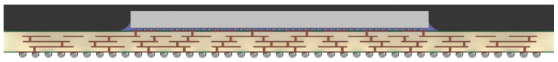
Bare die PoP



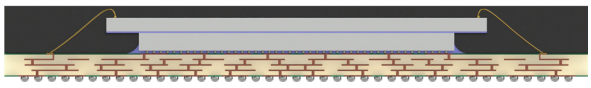
Molded PoP



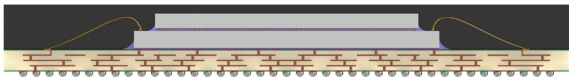
TMV® PoP



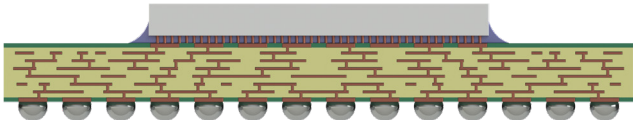
fcCSP



FlipStack® CSP



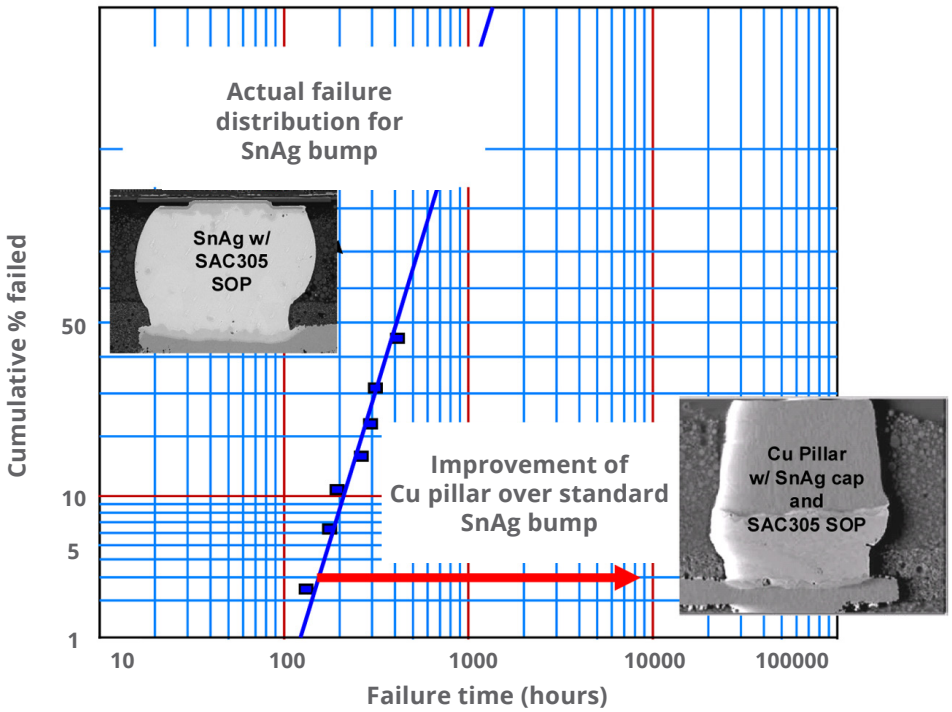
F2F FlipStack® CSP



FCBGA

Copper Pillar

Electromigration Reliability Comparison of Cu Pillar With SnAg Bump



The above plot shows improvement in life for Cu pillar over SnAg bump for the same current/temperature condition and similar bump/UBM geometry. No failure was observed in Cu pillar bump even after 8000 hours of testing at the same condition.

SQB Results

Test	Test Conditions	Read Point	SS	Results
MSL3	30/60-192	260°C 3x	77 x 12 Lots	Pass
T/C B	-55°C/+125°C	1000x	77 x 3 Lots	Pass
HAST	130°C/85% RH	96 Hrs	77 x 3 Lots	Pass
T&H	85°C/85% RH	1000 Hrs	77 x 3 Lots	Pass
HTS	150°C	1000 Hrs	77 x 3 Lots	Pass

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