X2FBGA: a new wire bond CABGA package

By Yeonho Choi, Burt Barber [Amkor Technology, Inc.]

The wire bond ChipArray® ball grid array or CABGA package provides versatile solutions for a broad array of semiconductor products used in a variety of automotive, industrial, computing, networking, consumer and mobile applications. In addition to offering high performance and flexible signal routing capability for high I/O count devices, the CABGA family of small footprints and thin form factors make it a member of the so-called near-die size packaging category for single-die products in the semiconductor industry. Ever-expanding capabilities in mobile handsets have always required a continuous reduction in the form factors for all semiconductor components: both footprint and height.

The most recent CABGA achievement is the development of a maximum 0.4mm height fine-pitch ball grid array (FBGA), called X2FBGA (**Table 1**) to denote a double extremely thin FBGA form factor. X2FBGA's advantages offer it a potential position among the various near-die size packaging options available in the market, such as the quad flat no-leads (QFN) package, routable QFN package, flip-chip chip-scale packaging (fcCSP) and wafer-level packages. However, to overcome key challenges, specific actions had to be taken to make the assembly process feasible and bring solutions to market.

Identifying the challenges

Today, many packages can achieve a total seat profile less than 0.4mm including QFN, wafer-level packaging (WLP) side, fan-in WLP (also known as die size BGA or DSBGA) and fcCSP. The fan-in WLP height is determined by the wafer backgrind thickness during the backend process, so it is relatively easy to achieve. For QFN packages, mold cap tooling determines the body profile. With 0.25mm mold cap tooling, which has been commonly used for several years, only the lead frame thickness needs to be included. The fcCSP uses exactly the same package outline platform as the wire bond CABGA and it enables more complicated interconnecting options and higher I/O count with high efficiency and superior electrical performance. The fcCSP has the option to expose the die backside on top of the package, so its thinness control is a relatively easy way to offer a maximum 0.4mm profile.

Compared to other packages, wire-bond CABGA has more challenges to achieve a thin package profile. The added height of the CABGA solder ball bumps requires thinner die and ultra-low wire looping controls to fit all z-dimension stack-up elements within the thin mold cap space. The extremely-thin fine-pitched BGA (XFBGA) provides a maximum 0.47mm (or 0.50mm) height physical profile dimension, and, until recently, it has been the thinnest wire bond BGA achievable using traditional face-up die bond, wire connect and molding process technology combined with a commonly available thin 2-layer laminate substrate. Based on XFBGA thickness reduction, CABGA's miniaturization capability, approaching the IC die size, has been improved by tighter control of the die edge to the bond ring and the tighter clearance control of the die-to-package body edge. This extended miniaturization capability is essential for the wire bond CABGA package to expand its applications in various market sectors, especially in mobile devices.

Table 2 shows packaging options with maximum I/O and maximum profile thickness capabilities. The 2~7mm

	LFBGA > 1.2 mm	TFBGA ≤ 1.2 mm	VFBGA ≤ 1.0 mm	WFBGA ≤ 0.80 mm	UFBGA ≤ 0.60/0.65 mm	XFBGA ≤ 0.47/0.50 mm	X2FBGA ≤ 0.40 mm
	CA-lfBGA	CA-tfBGA CTBGA	CA-vfBGA CVBGA	CA-wfLGA CA-wfBGA	CA-ufLGA CA-ufBGA	CA-xfBGA CA-xfLGA	CA-x2fBGA CA-x2fLGA
Mold Cap	0.70 mm 0.95 mm	0.60 mm 0.53 mm	0.45 mm 0.53 mm	0.45 mm 0.35 mm	0.35 mm 0.25 mm	0.25 mm 0.20 mm	0.1x mm
Substrate Layer	2, 4 or 6 Layer	2 or 4 Layer	2 or 4 Layer	2 or 4 Layer	2 or 4 Layer	2 Layer	2 Layer

Table 1: Amkor's ChipArray® BGA offerings: low-profile fine-pitch BGA (LFBGA), thin-profile fine-pitch BGA (TFBGA), very fine-pitch BGA (VFBGA), very very thin-profile fine-pitch BGA (WFBGA), ultra-fine BGA (UFBGA), extremely-thin fine-pitch BGA (XFBGA), and the newest X2FBGA.

Wafer Level Package (Fan-in & Fan-out) / Laminate fBGA / 1 Layer routable CSP, Additive / 1 Layer rt MLF (2 row IO + P*, 3rd exp pw bar*) Subtractive / Dual row MLF / Single row MLF					Possible BGA with under Die Area IO		Max 4 row IO depth Assumed		HVM max (& theoretical full array)		Full array Bump Assumed / Thickness per DPS Backgrind, 0.15~0.4mm wafer + bump		2L Wire bond fBGA thickness in production				1L rt CSP rt MLF		MLF/LGA		
Foot print	0.5mm Pitch	0.4mm Pitch	0.35mm Pitch	0.5mm Pitch	0.5mm Pitch	0.4mm Pitch	0.5mm Pitch	0.4mm Pitch	0.5mm Pitch	0.4mm Pitch	0.35mm Pitch	0.3mm Pitch	max 0.8 WFBGA	max 0.6 UFBGA	max 0.5 XFBGA	max 0.47 X2FBGA	max 0.8 LGA	max 0.50 LGA	max 0.40 LGA	max 0.8 LGA	max 0.50 LGA	max 0.35 LGA
2x2	8	12	16	NA	16	16	16	16	16	16	25	36										
3x3	16	20	24	NA	28	36	36	49	36	49	64	81										
4x4	24	28	32	NA	44	52	64	80	64	81	121	169										
5x5	32	40	44	44/52	60	72	81	112	81(81)	144(144)	192	256										
6x6	40	48	56	60/68	76	88	112	160	121(121)	155(196)	264	360										
7x7	48	60	68	76/84	88 + P	112 + P	144	192	169(169)	211(289)	400	484										
8x8	56	68	80	84/100	104 + P	128 + P	176	240	225(225)	308(361)	484	676										
9x9	64	76	92	100/116	120 + P	152 + P	208	272	265(289)	383(484)	625	841										
10x10	72	88	104	116/132	134 + P	168 + P	240	320	346(361)	454(576)	784	1089										
11x11	80	100	112	132/148	152 + P	192 + P	272	352	416(441)	486(729)												
12x12	88	108	124	148/164	168 + P	208 + P	304	400	424(529)	745(841)												

Near Die Size Package Sweet Spot

Table 2: Near-die size packaging I/O density options and sweet spot analysis.

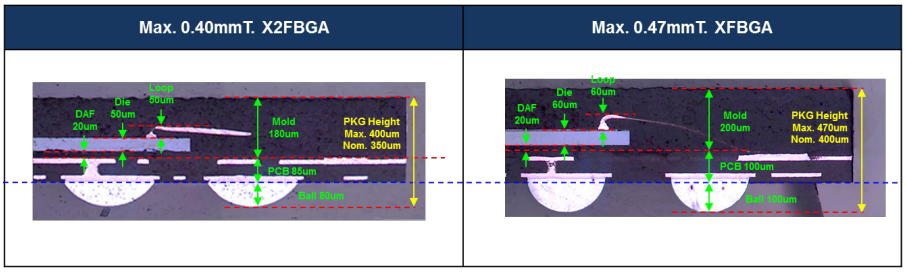

Figure 1: Cross-sectional comparison of the XFBGA and X2FBGA packages' construction.

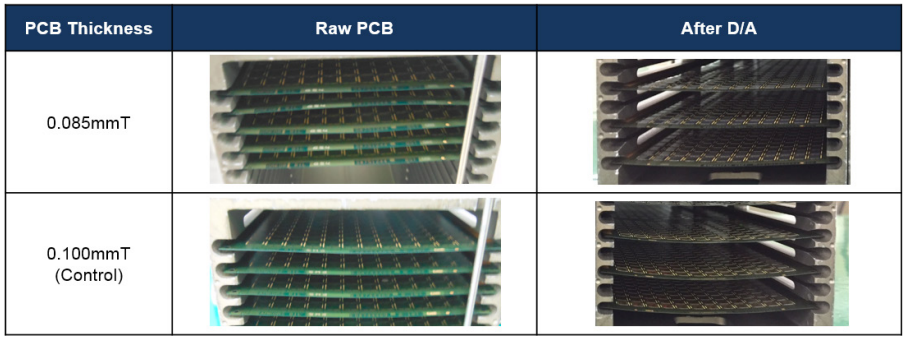

Figure 2: Substrate in the front-end-of-line (FEOL) process magazine, showing deflections and warpage management.

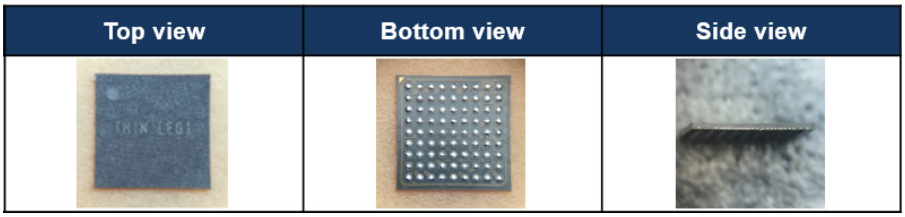

Figure 3: X2FBGA picture after finishing the assembly.

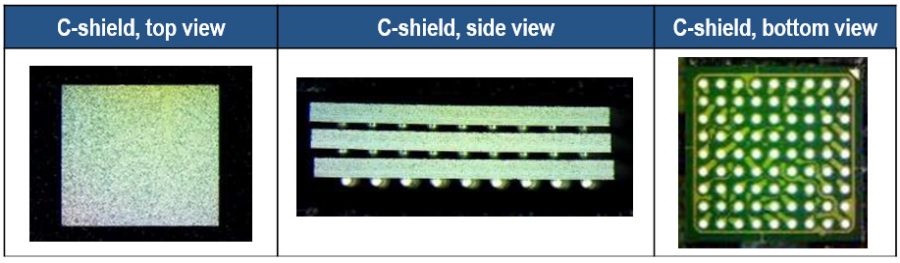

Figure 4: X2FBGA after conformal shielding.

body size range could be the sweet spot of the market opportunity that wire bond CABGA packages can contribute considering today's die size and I/O number trend. Taking these factors into account, wire bond CABGA packaging is expected to have significant acceptance and contribute to further growth in this market with continued miniaturization in the near-die size packaging field. To achieve a near-term product, the maximum 0.40mm profile wire bond CABGA process capability was targeted. The main technical challenges in this development occur in four key areas: design, material, process and method.

Addressing the challenges

Designing the cross-sectional structure and its geometrical details, as well as setting control limits during substrate manufacturing and IC assembly processes, are the foundations for successfully building the X2FBGA. These areas establish the goals of each process and provide the targets to reach. To achieve the final maximum 0.40mm BGA height including tolerance limit, the nominal z-height dimension must be reduced; 0.35mm was set as a final nominal dimension target to allow a +0.05mm tolerance specification limit. Compared to the existing XFBGA (see **Figure 1**), this required a 28% tightening of overall tolerance in addition to a 12.5% reduction of actual packaging material thickness. Mold tool design, substrate tolerance, and the associated design features to control bump ball height are all required to adjust, tighten and meet the target thickness reduction.

Material selection for mechanical property management is another challenge. The substrate core and solder mask material selection must be stiff enough to withstand and maintain the flatness of the substrate throughout the assembly process. Lower coefficient of thermal expansion (CTE) and ultra-thin (40µm) core material combined with a low-CTE solder mask is required to control the deflection and deformation of the raw PCB substrate and after-bake die attach (D/A) (see **Figure 2**).

The mold compound's physical properties were studied and chosen to prevent the molded strip warpage and maintain high quality and productivity during the backend of the assembly process. Wafer thinning and strength management, including sawing methods, are also important. The 50µm wafer thickness and die handling are performed to prepare for subsequent assembly processes. With this construction, the die top to mold cap leaves a z-space of only about 110µm. In addition to the ultra-low wire looping control during the wire bond process, the review and control procedure of the markable area on the body top surface must be considered during production planning to prevent potential interaction of the laser mark engraving depth with wires. **Figure 3** shows the end results.

A micro solder ball formation process with 80µm or less bump height has been in high-volume manufacturing for many years. Its production capabilities and market acceptance are well established for WFBGA and UFBGA packages. However, in some applications, customers specify a nominal 100µm bump height as the de facto application requirement. To prepare for and address such an application requirement, an additional 10-20µm of tooling reduction and

adjustment in mold tool and die thickness have also been provided to allow additional bump space in the final package.

To certify its volume production readiness level, the X2FBGA package has been subjected to an internal qualification procedure and reliability tests. With all testing completed, the X2FBGA package passed all qualification requirements. Because this package targets mobile device applications, a conformal electromagnetic interference (EMI) shielding process is offered as an option. The BGA form adds challenges in shield coating because the ball bumps require masking to prevent coating material contamination on the bottom side. As a result of targeted efforts in process development for a micro bump BGA conformal shield, we now offer a shield process up to a 100µm bump height BGA (see **Figure 4**).

A new design option

By studying where and how the wire bond CABGA can provide advanced miniaturized packaging solutions, design, process, bill of material (BOM) and method advancements have been developed and implemented into Amkor's manufacturing processes to offer the X2FBGA package's capabilities. Ultra-thin substrate design, sourcing, the right assembly material selection, tooling and process combinations are all available to support a variety of needs. We encourage users to consider the X2FBGA (with other advanced packaging options based on pros and cons) for their IC packaging needs and take advantage of its capabilities to satisfy existing and emerging design requirements.

Acknowledgement

ChipArray is a registered trademark of Amkor Technology, Inc.

Biographies

Yeonho Choi received his BS degree in Chemistry from Ajou U. in Korea, and is Director, CA Laminate Products at Amkor Technology, Inc.; email Yeonho.Choi@amkor.com

Burt Barber received a BS degree in Electrical Engineering from Santa Clara U. and an MBA from the U. of San Francisco. He is Sr. Director, CA Laminate & PBGA at Amkor Technology, Inc.