Test Flow for Advanced Packages (2.5D/SLIM/3D)

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Abstract

With the newest integrated circuit (IC) packages, the old adage of “faster, cheaper and better” (FCB) gets an additional adjective - “slimmer.” This generates the new term “faster, cheaper, better & slimmer” (FCBS) that should become a new industry buzzword. With FCB, it was a generally accepted principle that one could get “two out of the three.” However, with the FCBS concept, it is understood that the combined product will exhibit all four characteristics with combined benefits that outweigh the sum of the individual components.

Product designers cognizant of the FCBS requirements are pushing outsourced assembly and test (OSAT) companies to deliver integrated modules (chips) that do more, with a thinner form factor. This includes integrating devices into a package, creating a System in Package (SiP), which combines devices from different technology nodes. Such integration has been made possible by the use of advanced substrates that provide fine line and space, or with the use of silicon interposers that use Through Silicon Via (TSV) technology. Alternatively, product integrators can use Amkor’s most advanced packaging solution, Silicon-Less Integrated Module (SLIM™) technology that eliminates TSVs, further reducing package height. Die stacking technologies including 3D and package stacking approaches such as Package-on-Package (PoP) are also employed to deliver FCBS products.

One important aspect of achieving an FCBS product is reducing scrap cost. This is achieved by an interactive test flow, wherein the device (system/ sub-system) being built is tested as individual components as well as tested during the assembly process. Testing partially assembled devices poses new challenges and risks, such as handling thinned dies and exposed pads. This paper examines the various test insert points and proposes a suitable test flow for products that use advanced packaging technologies.

Test Flow for Advanced Packages (2.5D/SLIM/3D)

The process of building a “chip” can be viewed as a fan-out process, where the die is attached to a substrate or interposer, which provides electrical connectivity from the enclosed die to the outside world. The substrate converts the die’s fine pitch and small pads to a pad size and pitch that can be easily assembled on a printed circuit board. In the case of a multichip module, the substrate or interposer also provides electrical connectivity to other dies on the interposer or substrate. Typically the substrates are electrically tested by the substrate manufacturer and only known good substrates (KGSu) are shipped to the OSAT. In the case of a 2.5D interposer, since the interposers are shipped to the OSAT as full thickness wafers, top to bottom connections on the interposer can only be checked after the wafer is thinned and TSVs are exposed. In the case of 3D chips, known good die (KGD) are stacked and bonded over each other. However, in the case of SiPs, either KGD or known good devices are populated onto the substrate or interposer.

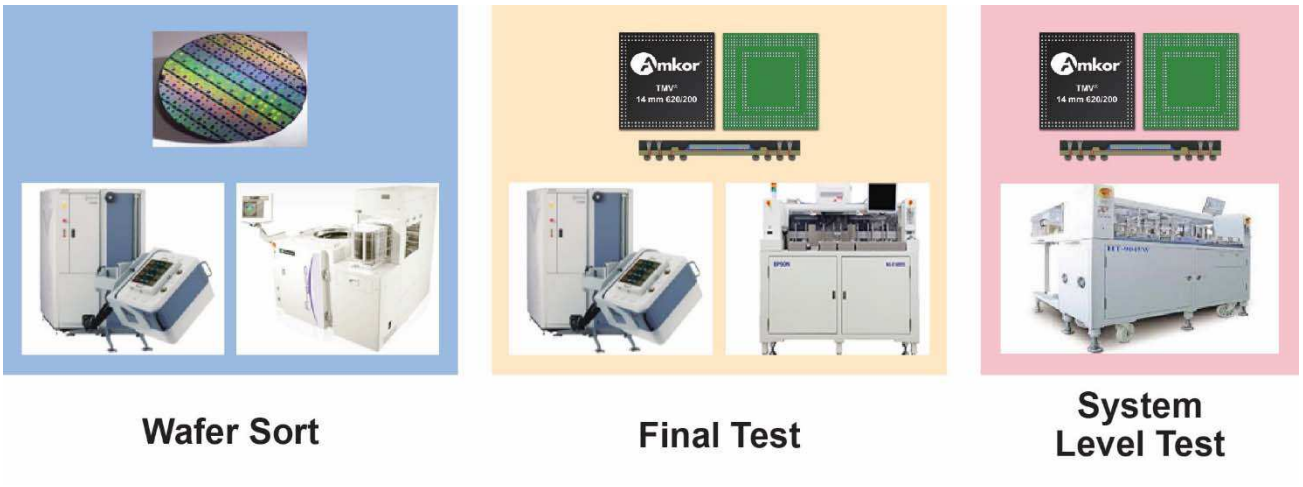

Figure 1: Traditional Test Insertion Points for Semiconductor Test

As shown in Figure 1, the standard test insertion points during traditional semiconductor test at an OSAT are Wafer Sort (WS), Final Test (FT) and, in some cases, System Level Test (SLT). At Wafer Sort, OSAT’s use automated test equipment (ATE) and automated probers that handle full thickness wafers (~800 µm). Here devices are tested for functionality rather than performance. After

all the assembly is completed and the device is in its final form, the device is sent for FT. During FT, the device is tested for performance using the minimum datasheet specifications as the lower limit. Devices that are targeted for specific applications in a reference design environment undergo SLT.

Improving Interposer Yield using Redundancy - Eliminating the Need to Test

The interposer wafer may consist of two or three metal layers, usually built using mature process node technologies such as 90nm or 65nm. These proven technologies provide highly reliable connections between dies and from die to the TSVs. The potential risk in connectivity can occur if the interposer has non-uniform TSVs. For example, if a single TSV were used to make a connection between the front side metal and the backside C4, and if this TSV's height were 10 µm shorter than the rest, no connection would result. However, adding multiple (one or more) redundant TSVs for each C4 connection, as shown in Figure 2, significantly increases the yield to the point where testing may not be necessary.

If a customer deems interposer testing necessary, they add daisy chain structures at certain strategic locations. Testing is usually done from the C4 side, where the pad diameter is 80 µm and the pitch is 120 to 150 µm, allowing for simple cantilever probe cards for test. During interposer test, if an open is detected in any of these test structures, the interposer die is marked as bad (unusable).

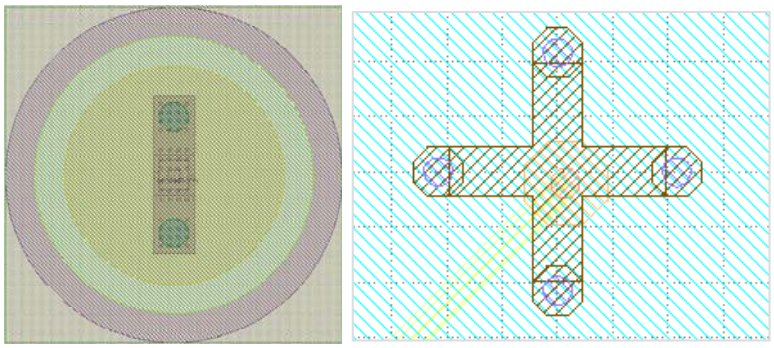

Figure 2: Redundant TSVs to C4 connection

Test Challenges with Advanced Packaging Technologies

When the goal of an advanced package is to have high performance at a lower power budget, the test requirements get pushed from "sub-speed testing" to "at speed testing." Now the device has to be tested for performance at the speed at which it is designed to operate and not a fraction of its operational speed. This offers new challenges – such as making electrical contact, high-speed performance of the probe card, high-current consumption of the device (at probe), bare-die handling and heat dissipation (see Figure 3).

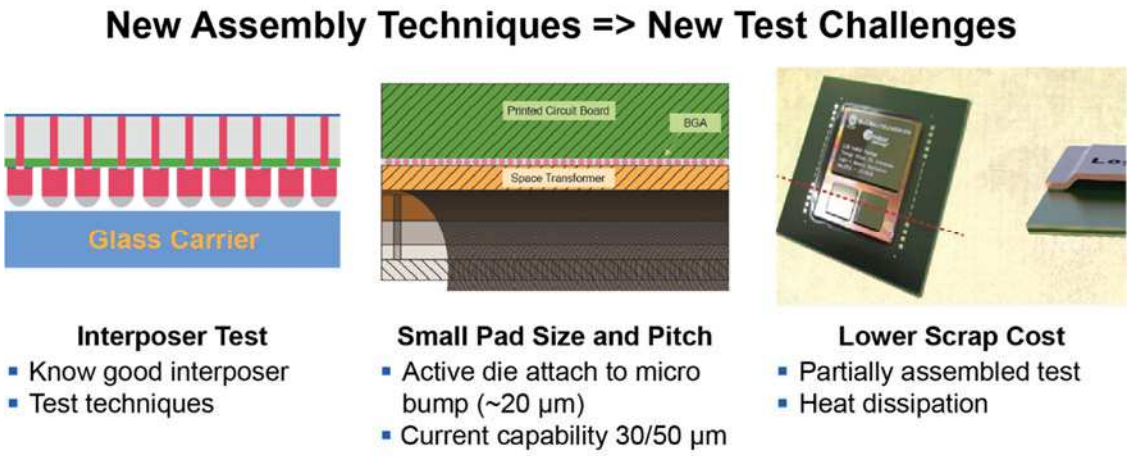

Figure 3: New Assembly Techniques provide New Test Challenges

To maintain signal integrity at high speeds, large sacrificial pads are replaced with small pads that attach to the micro-bumps. The number of pins that make contact with the probe card can be in the range of 20,000. With a 5-gm force per probe needle, the probe card core can experience over 100 Kg of force, making it susceptible to bending and reducing planarity. Furthermore, device operating currents could well be in the 10's of amperes range, limiting the choice of needle technology. Running the device at speed, while checking for performance, creates large amounts of heat. To prevent thermal runaway, the die is tested at subzero temperatures requiring special gaskets to prevent condensation and water/ice buildup on the tester-prober interface.

When devices are built using the advanced packaging technologies with multiple components, each with a yield Y_i, the combined yield can be represented as:

$$Y_{combined} = Y_{substrate} * Y_{interposer} * Y_{die1} * Y_{die2} * Y_{die3} *\ldots.$$

In such cases, where multiple dies are added to a device, it becomes necessary to test the partially-assembled device after each die is added to the build to reduce scrap costs. For economic reasons, OEMs may opt to skip testing the partially assembled units, when components of very high yield are added to the build.

Testing partially assembled devices at FT and SLT while operating at full speed brings new challenges to test, such as handling partially assembled units with exposed die. The risks added by testing at this stage are chipped edges, cracked die or cracked packages. To keep device temperatures under control, active thermal control systems are connected to chiller units to maintain constant device temperature. Additionally, partially assembled devices require electrical insulation to prevent shorting of exposed pads and the chuck during test.

Adapting Existing Equipment for Advanced Package Test

When testing advanced packages, OSATs prefer to leverage existing assets rather than invest in one-of-a-kind testers or material handlers (see Figure 4). For interposer testing, the incoming requirement at test is to have the thinned 100 µm interposer wafers mounted on a 700 µm glass carrier. This allows standard probers to handle the interposer wafer as a full thickness wafer.

Testing active dies with small pad sizes and pitch, requires probers with 1 µm accuracy and the ability to apply up to 400 Kg of force. Thermal control of the die is achieved by adding the optional chiller units to the prober that allow the chuck temperature to be lowered to -40°C.

Standard handlers are equipped with active thermal control (ATC) heads with each head having its own heater / chiller unit. In more sophisticated implementations, the active thermal control

unit is controlled by the test program which reads the die temperature and regulates the ATC behavior. The thermal chuck design has to be optimized to avoid pushing down on passives, making contact with exposed pads and applying uniform pressure on the exposed dies.

Figure 4: Test Insert Points for Advanced Packages

System Level Tests are usually performed on asynchronous handlers – meaning, each site test state is independent of the other. Asynchronous handlers allow a device that has failed a test to be removed and placed in the output tray and a new device inserted into that test socket. In addition to the modifications needed for device handling and ATC, SLT requires hard disk duplication - maintaining the same BIOS version and motherboard hardware versions across all test sites. SLT executes the complete boot sequence and therefore results in long test times (90 to 300 seconds). Long test time mandates high parallel testing to meet throughput requirements. It is common to run 12 sites in parallel using asynchronous handlers. In these systems, each site has its own tester, which replicates the target application. This tester could be a PC for a CPU/GPU application or a cell phone board for an applications processor. The key to successful SLT operations lies in the design on the test executive that controls and communicates with each individual test site, consolidates test data files and issues commands to the handler.

Universal Test Flow for Advanced Packages

Despite the differences of the build technique employed with SLIM, 2.5D or 3D, the test flow in Figure 5 defines the universal test flow that can be taken when building such devices. The test stages are green boxes, while the assembly / middle end of line (MEOL) processes are shown in black. The incoming and outgoing from the OSAT are shown in blue. The red boxes define the test equipment used at each stage with a description of the process or test stage.

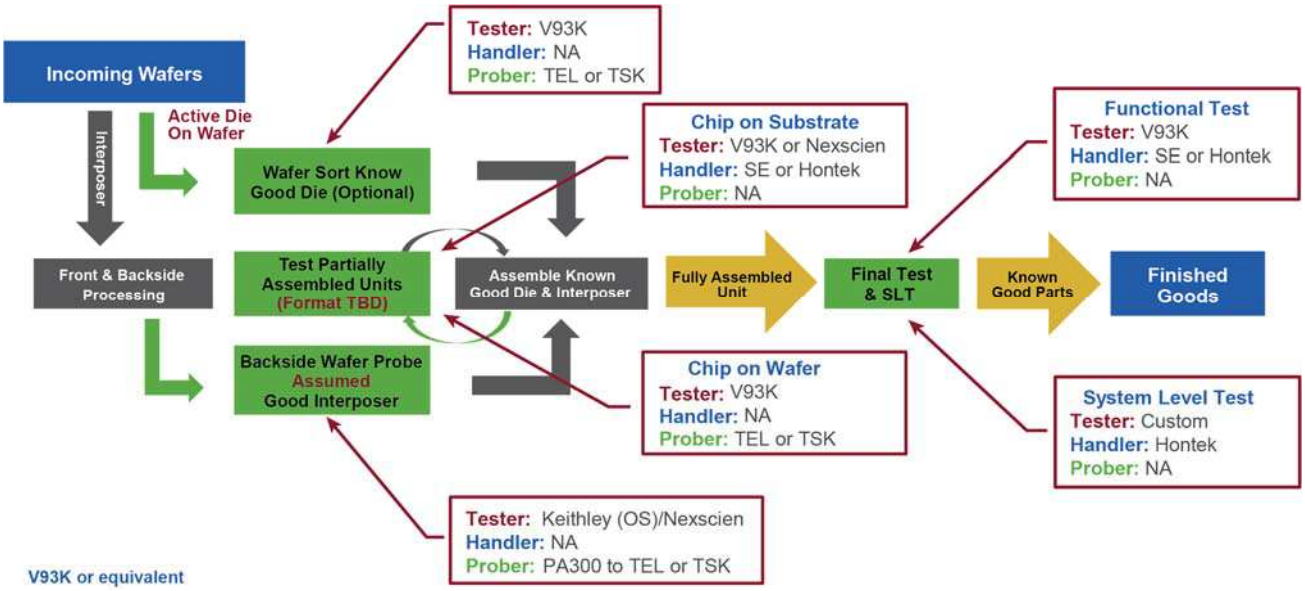

Figure 5: Test Flow for Advanced Packages

Incoming wafers have two alternate test paths: active wafers are tested as full thickness wafers and passive interposers with test structures are tested after thinning and mounting on a glass carrier wafer. If the interposer wafer is tested on an automated prober with a wafer loader, care must be taken to ensure the prober recognizes the notch on the wafer for orientation. During interposer test, only the test structures' connectivity is verified, and if found good, all interconnects on the interposer die are assumed good.

Known good die and assumed good interposers are assembled and the partially assembled unit is sent to test. Depending on the test criteria, the tests can be either opens/ shorts to verify connectivity or functional tests to check for performance variations. When there are multiple dies on a single chip, after each die is attached, the partially assembled unit is tested. The form factor at test will depend on the assembly technique i.e., Chip on Substrate (CoS) or Chip on Wafer (CoW). In the case of CoW, the material hander is a prober, while in the case of CoS, a final test handler is employed. This process of partially assembled testing continues as new dies or devices are added to the unit being built. In the case of CoS, the customer may request that the partially assembled unit be tested on SLT.

After full assembly, the unit is tested using ATE and, in some cases, is sent to SLT. If the device is equipped with non-volatile RAM, tracking information such as wafer number, lot number, die x, y, etc. are written to the device during test, enabling unit level traceability. In some cases, the device is marked with a 2D barcode that can be scanned to derive the unit level information.

Conclusions

Advanced packages that use SLIM/2.5D or 3D assembly techniques tend to pack high performance while consuming lower power into a smaller and slimmer package. Each die in the package in itself is a high performance unit. Integrating these individual dies into a single package provides improved performance greater than the sum of the individual components if packaged separately. With the addition of each individual die to the package, the cost of the package increases. Therefore, it is absolutely necessary to test each individual die for performance prior to assembly and test the partially assembled units during the assembly process to minimize scrap costs. Furthermore, with appropriate analysis and package partitioning, each classification of package or subassembly can be tested in a universal test flow to satisfy the most stringent criteria.

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