A PRACTICAL APPROACH TO TEST THROUGH SILICON VIAS (TSV)

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ABSTRACT
There is increased interest in developing packaging solutions that provide higher bus speeds at reduced power per bit ratios. This has driven designers to look for techniques that shorten the distance between chips (reducing drive currents) and use wider data busses (finer line-space traces) resulting in the growth of two and a half dimension (2.5D), and three dimensional (3D) packages. While much of the effort and attention has focused on the development of processes and technologies to build Through Silicon Vias (TSVs), the industry has lagged behind in developing test strategies to qualify these designs.

Electrical testing of TSVs can only be performed after back grind and etch processes expose the TSVs - a task that is usually performed at the Outsourced Assembly, and Test (OSAT) supplier, see Figure 1. Therefore, when a TSV interposer wafer leaves the foundry, the quality of the TSVs remains unknown until it is processed at the OSAT.

Within a package, the functions of the TSVs can vary widely. Basically, they may be used to carry DC current to power the chip or carry high-speed signals for input /output (I/O) pins or provide low-impedance paths which connect the die to the ground plane. Based on their functions, specific tests need to be performed to verify TSV functionality. Furthermore, TSVs need to undergo characterization tests such as stress and electro-migration to quantify their long-term reliability.

This paper analyzes the different kinds of tests that should be performed on TSVs during the design, qualification and production phases. It provides a case study to an interposer vendor qualification and analyzes the data collected in the process through various laboratory experiments. Additionally, it also discusses the practical challenges faced while testing TSVs on thinned wafers, including the limitations of equipment and probe card capability.

Keywords: Through Silicon Via, TSV, Test, OSAT, TSV redundancy.

INTRODUCTION
Defects in TSV structures are potentially caused during their manufacture at the foundry or during the TSV "reveal process" at the OSAT. During the fabrication of TSVs, micro-voids, due to quasi-conformal plating, might lead to weak-opens in TSVs, while ineffective removal of the seed layer might lead to shorts between TSVs [1].

A wealth of work [2-5] has been done in testing the quality of an interposer after active-die or dies attachment. These techniques include Built-In-Self-Test / Diagnosis / Repair (BIST/D/R), Reduced Pad-Count Testing (RPCT), Test Data Compression (TDC), etc. If a problem with a certain path is identified, these approaches rely on redundant resources that can be used to restore device functionality. However, problem identification occurs after an expensive Application Specific Integrated Circuit (ASIC) has been attached to the interposer / substrate. If these techniques are used when the first die is attached on a multi-chip module, they can detect problems early in the assembly process. At this point, testing can identify if the problem can be fixed by using an alternate electrical path, apply the fix, then verify the fix or if no redundancy exists, fail the subassembly before more dies are added, reducing scrap costs.

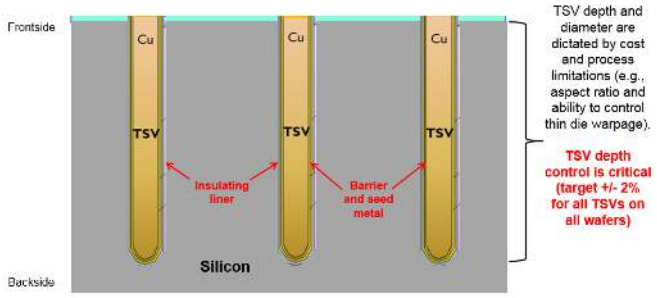

Figure 1: Interposer wafer with TSVs as received from fab

Often, the ASIC used with the TSV interposer is a large die, which typically is a high end processor, with about 60% to 70% of the dies per wafer meeting the performance criteria of the final package. Utilizing one of these premium ASICs to identify a fault in the interposer is an expensive option and not the optimal use of a scarce resource – the ASIC.

To achieve the lowest scrap cost, methods of testing the interposer die before it is attached to a substrate should be explored. An easier approach, but at a slight higher cost, would be testing the interposer vias after it is attached to the substrate.

Alternatively, the interposer designer can use multiple redundant vias “n+1”, where “n” represents the number of redundant vias for a single vertical connection. This method works well when there is adequate space under the ASIC, however, as the size of the die shrinks, the number “n” tends to zero i.e. no redundancy, leaving space only for a single via per connection. Furthermore, current trends in the reduction of pad size and pitch might limit the ability to

place redundant TSVs for each connection. Therefore, it is necessary to establish robust manufacturing methods for TSVs that result in ultra-high yields.

POTENTIAL DEFECTS DURING TSV MANUFACTURE

According to Nova Measuring Instruments [6], the first phase in the TSV process, i.e. via formation, lays the foundation to the success or failure of the entire process. The subsequent steps of insulation and metallization, as well as the eventual thinning of the wafer to expose the buried TSV, depends on the height uniformity and the shape of the etched via. Therefore, it is critical to closely monitor these two parameters including: depth, side-wall slope, top and bottom diameters (CDs), and bottom curvature during the manufacturing of the interposer wafer.

The TSV metrology challenges include:

- Control of via insulation thickness and integrity.
- Control of voids and seams in the metallization phase.
- Control of in-via defects, random and systematic.
- Control of wafer thinning, TSV reveal, and back-side passivation.

Optical Inspection at the foundry

Optical inspection has the advantage over electrical test since there is no physical contact to the pads and it can identify faults that may not be otherwise detected. However, optical inspections using infrared (IR) photo emission microscopy or Dark-Field Reflectometry, etc. [7] are techniques that can be used at the foundry and are outside the scope of this paper, which focuses on tests that can be administered after the TSVs are revealed at the OSAT.

TSV FABRICATION PROCESS AT OSAT

The least-cost route to implementing electrical test for TSV interposers would be inserting electrical test in the fabrication process of the interposer without breaking the existing flow or by finding an appropriate slot in the assembly flow where the test can be inserted with minimal disruption.

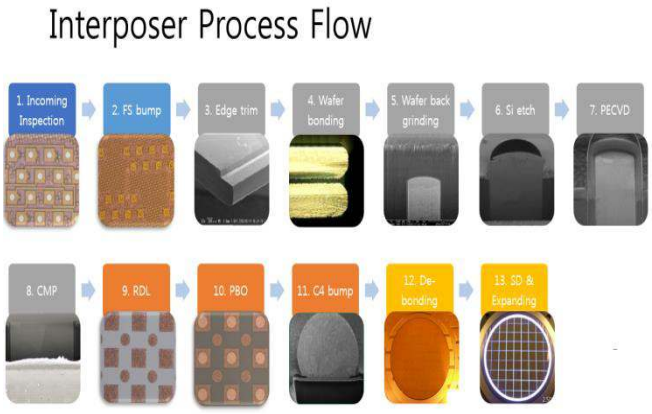

Figure 2: TSV interposer process flow

A typical TSV interposer process flow is shown in Figure 2. The color coding of the tabs follows these rules:

- Steps 1 and 2 are completed at the bump facility;
- Steps 3 to 8 are referred to as “Middle-End-Of-Line 1" (MEOL 1) process;
- Steps 9 to 11 are performed at the bump facility,
- Steps 12 and 13 are referred to as " Middle-End-Of-Line 2" (MEOL 2) process.

As seen in Figure 2, the TSVs are exposed after step 8.

Optical Inspection at the OSAT

At the OSAT, defect identification can be performed either optically [7] or through electrical tests. Optical inspection can be performed at the OSAT after step 8 in the TSV manufacturing process (Figure 2). At this point in the TSV flow, the TSV is exposed and the TSV diameter should be within the set limits. As shown in Figure 1, the TSV depth control is suggested to be within ±2% of the TSV height.

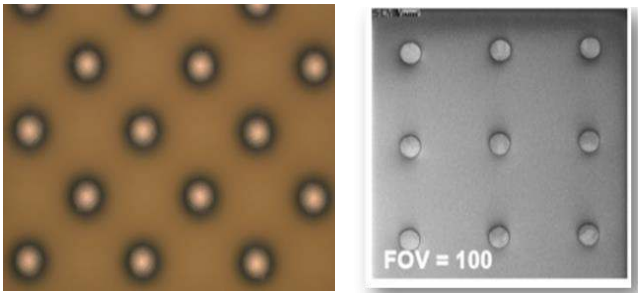

Figure 3: A picture of an array of the revealed TSVs

Optical inspection is the first coarse test step with 100% inspection of the revealed TSV’s shape, size and color which determine if the TSV is good.
Automatic optical inspection (AOI) machines can be programmed to identify the absence (no reveal, i.e., too short a TSV) and to measure the diameter of the revealed TSVs. If the diameter measured falls outside acceptable limits, it would indicate that the TSV formed is not of the expected cylindrical shape. In both cases, the associated die will be graded as defective.

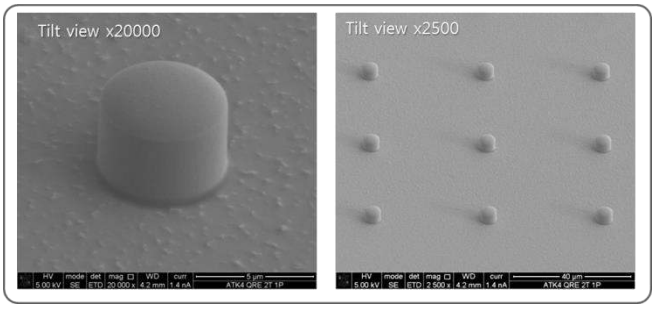

Figure 4: TSVs protruding from the wafer backside after *primary* reveal

Post step 12, the wafer is de-bonded from a carrier and mounted onto a film frame. Electrical testing of the interposer wafer is best handled when it is still mounted to

the carrier since this allows the use of standard wafer probers during testing. This limits the possible choices for interposer testing between steps 10 and 11 or 11 and 12. The optimal position for test would be after the completion of the controlled collapse chip connection (C4) attach, intercepting the wafer after leaving the bump facility and before entering the MEOL 2 process, while paying close attention to cause little or no damage to the C4s during the test. Equipment is being developed to handle thinned die that will be picked up from a waffle pack. When this is available, it may offer more options for test.

Electrical Test at OSAT

Since the function of the interposer is to make an electrical connection from the front-side micro bumps to the back-side C4s, one would expect electrical testing of the interposer to measure continuity from the micro bumps to the C4 bumps. While there is equipment capable of performing double-sided probing [8] i.e., make simultaneous contact with pads on the front and back side of the wafer, such equipment is not common inventory on OSAT test floors. Using stock equipment found at OSATs can help further reduce the cost of test. Standard probers make electrical contact with only one side of the wafer. To test top-to-bottom connectivity, daisy chains test structures that traverse the top and bottom of the die shown in Figure 6 are used to verify TSV quality. Testing is done on the C4 side where the contact diameter is typically in the 80 µm to 120 µm range allowing for less-expensive probe cards.

CASE STUDY: TSV SUPPLIER QUALIFICATION

A test vehicle (Figure 5) which resembles the final product interposer allows its use for both interposer vendor qualifications as well as the package-assembly process qualification. This would imply that the test vehicle and the final product would share the same physical size, quantity, and location of the micro bumps / C4s. A good practice is to have the test vehicle wired with multiple daisy chain test structures, where each structure is a set of TSVs grouped by their position on the die (e.g. GPU1 NW Corner) with the goal for the daisy chain to flow through every single TSV in that area. Creating regions helps in the failure analysis team to zero-in on the fault area.

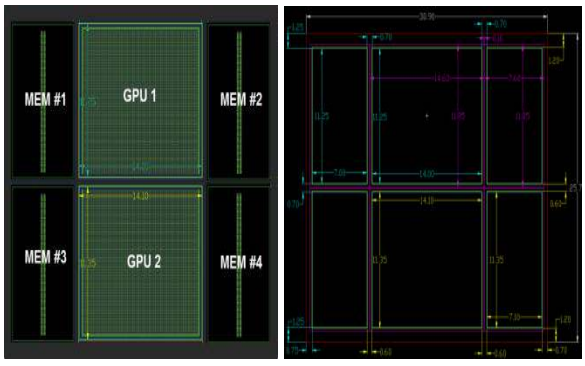

Figure 5: TSV interposer test vehicle

Interposer Designed for Test

As shown in Figure 5, the end product interposer design was translated into a test vehicle. With a micro bump size within the sub 25-µm range and a C4 size of around 80 µm, the final product accommodated approximately 75,000 micro bumps and about 25,000 C4s.

For versatility, the test structures were designed to break the daisy chains into sub-chains. The electrical path for each sub-chain would be completed by a metal layer on the interposer. Additionally, the sub-chains would be joined to form the full chain using metal layers from the top-die test vehicle, as shown in Figure 6.

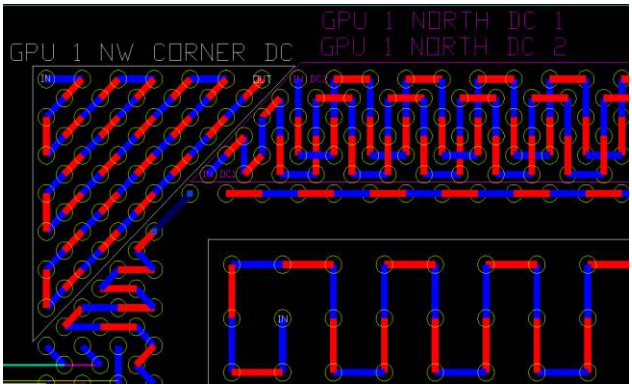

Figure 6: Daisy chain top die (red) and interposer (blue)

Additionally, the test vehicle was used to study the impact of stress and strains which the interposer die will experience when the package is fully assembled (i.e., with top dies attached, under-filled, stiffener ring attached, and the complete assembly over-molded, etc.), therefore, the location of the daisy chains was critical. Daisy chain structures were placed in areas where the large mechanical stress and strain affect the reliability of the TSV structures. Additionally, the test vehicle incorporated strain gauge structures, which was used to measured and monitor stress/strain on the package through the assembly process.

Daisy Chain Resistance Selection

The designer has to choose the resistance values of the daisy chains bearing in mind the metrology. From an equipment perspective, when the number of networks to be measured is below two dozen, a traditional ohmmeter can be used, however, when it exceeds a hundred, the choice of equipment switches to automatic test equipment (ATE) or open-short testers. The metrology ATEs use to test for opens or short is called force current, measure voltage (FIMV). They achieve this by setting the clamp voltage to 3V (adjustable) and forcing a current of 100 µA, then measuring the voltage between the pin under test and ground. The supply and ground pins are connected to ground. A voltage measurement between 0.2V to 0.8V (diode forward voltage) would indicate that the pin under test is connected to the silicon. An open would be indicated by a measurement of clamp voltage and a short (to VDD or GND) by a 0V reading.

Pair #	Test Name	C4 Pad (In)	C4 Pad (Out)	Distance between Test Points (um)	Group	Spec Limit (+/- 10%)	
						Lower	Upper
1	1VIA_NETWORK	A12	A9	540.00	1	54.61	66.74
2	2VIA_NETWORK	FY12	FY9	540.00	1	54.61	66.74
3	2VIA_NETWORK2	FY158	FY161	540.00	1	54.61	66.74
4	CONTROLVIA_NETWORK	A158	A161	540.00	1	54.61	66.74
5	CRACK_GPU1_NE	F123	G121	402.49	2A	12.62	15.42
6	CRACK_GPU1_SW	CG49	CH47	402.49	2A	12.39	15.14
7	CRACK_GPU2_NE	CN123	CP121	402.49	2A	12.68	15.49
8	CRACK_GPU2_SW	FP49	FR47	402.49	2A	12.62	15.42
9	CRACK_GPU1_NW	F47	H48	402.49	2B	12.62	15.43
10	CRACK_GPU1_SE	CF122	CH123	402.49	2C	12.69	15.51
11	CRACK_GPU2_NW	CN47	CR48	402.49	2C	12.62	15.43
12	CRACK_GPU2_SE	FN122	FR123	402.49	2C	12.71	15.53
13	NE_CORNER	A162	H169	1781.91	3A	53.47	65.36
14	SW_CORNER	FN1	FY8	1781.91	3A	53.47	65.36
15	NW_CORNER	A8	H1	1781.91	3B	53.47	65.36
16	SE_CORNER	FN169	FY162	1781.91	3B	53.47	65.36
17	TSV_CHAIN_GPU1	CF48	G50	10626.10	4	414.55	506.68

Figure 7: Test list, C4 pads and test limits

ATE machines complete the measurement in a couple of milliseconds and are not expected to provide an accurate resistance measurement, rather just provide a pass or fail result. Thus it is best for the designer to maintain the daisy chain resistance values between 300 ohms and 3 kilo ohms. Furthermore, most ATE tester configurations have up to 2500 pins available for test; therefore, the designer must balance the lengths of the daisy chain and the nets to within the tester pin counts.

Vendor Qualification – Test Metrology and Apparatus
One of the key requirements for the evaluation was to provide quick feedback on the quality of the interposer; therefore, it was decided co-locate test with the assembly line, limiting the equipment choice. The prober available on the assembly line was a semi-automatic PA300 with 12-inch wafer capability. The test setup, probe card, and test program had to be simple and intuitive for an operator to use and provide downstream feedback.

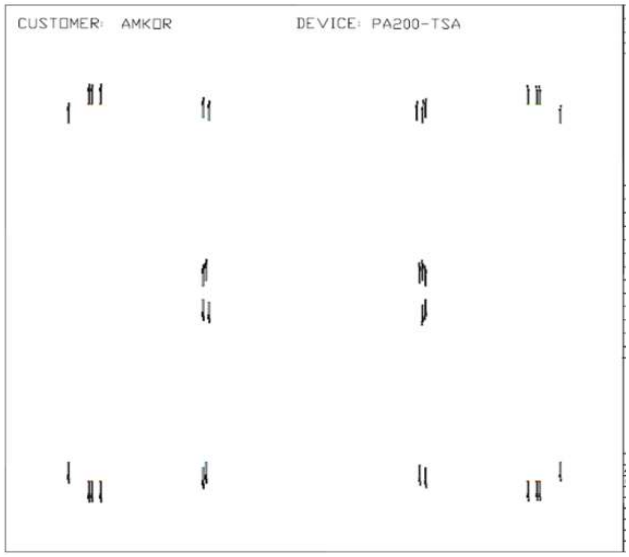

Figure 8: Probe locations for test vehicle

To limit the size of the experiment, seventeen test structures (Figure 7) were selected, located symmetrically in the four quadrants of the die (Figure 8). A cantilever probe card was used with four-wire capability, with two probes (force+ and sense+) landing on daisy chain input C4 bump, and two (force- and sense-) on the output C4 as seen in Figure 9.

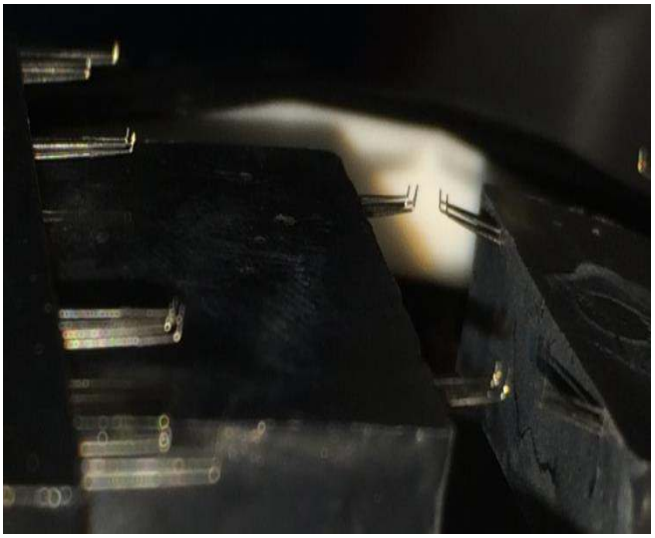

Figure 9: Cantilever probe card – zoomed in.

The test condition was "DC" only – i.e., resistance testing. High-frequency performance was done separately using 50-ohm co-planar waveguide test structures on the interposer and performed using a network analyzer. To avoid the additional, reflow step, the balanced contact force (BCF) was tuned to limit the damage on the C4 during probe [9], see Figure 10.

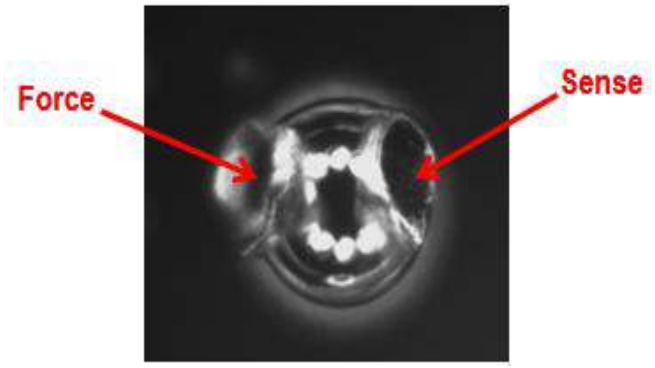

Figure 10: Scrub mark overdriven to show F/S

Using the interposer design information such as the trace width, thickness, and the daisy chain length, resistances for each daisy chain structure were computed, creating the test specification and the pass-fail limits. The test equipment consisted of four relay boards that switched the four-wire lines from the two Keithley 2400's source-measure units to two probe transition boards that mapped the measurement point to the probe needles as shown in Figure 11.

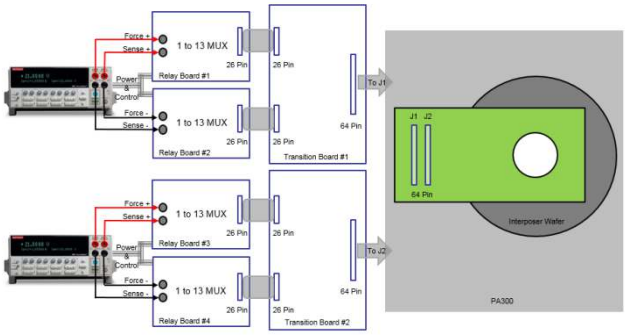

Figure 11: Test setup

Since a semi-automatic prober was used, the interposer wafers that were mounted on carriers were loaded manually on to the PA300 prober. The optical character recognition (OCR) feature was not available on the prober, so all carrier wafer IDs were manually recorded and later mapped to the interposer ID. Figure 12, shows an interposer wafer mounted on a carrier.

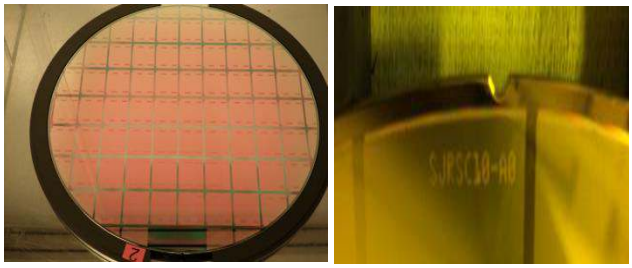

Figure 12: Interposer wafer on carrier

Test Data Resistance Measurements Interposer Rev# 1
In the first revision of 25 interposers wafers, the test data was collected and the measurement showed consistency across all wafers (Figure 13). Since the test structures chosen were symmetrical (Figure 8), it provided a way to compare the test structure results across the four quadrants of each die and with the wafer as a whole. From the histograms generated, the consistency within the datasets proved that both the measurement metrology and TSV manufacturing techniques were stable. Failures were observed at the outside ring of the interposer wafer (Figure 13). Within the die these failures were not limited to a particular area or test structure, but observed randomly distributed across the test structures.

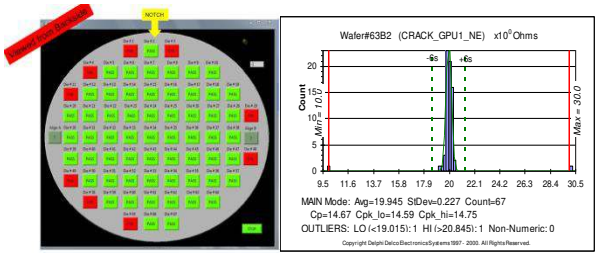

Figure 13: Wafer map and measurement histogram

An attempt was made to measure the leakage currents in the order of a few Femto-amperes on some of the test structures, but the 6-foot-long cables that connected the transition board to the probe card (Figure 14) proved to have a higher leakage than the 100 fA target measurements.

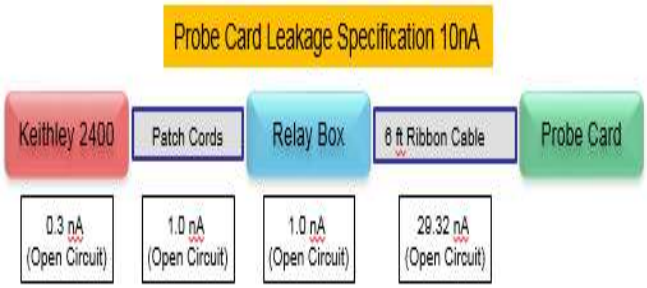

Figure 14: Open-circuit leakage measurements

This measurement could detect leakages in the order of a few of microamperes, identifying weak shorts. However, since substrates are considered "bad" only when its leakage currents exceeded 100 µA, setting fail criteria for the interposers a couple of orders of magnitude higher than the substrate it attaches to, would result in over rejection of interposer die. As a result, investing in a test setup to measure Femto-amperes of leakage did not justify the expense and was found unsuitable for high-volume production.

Test Data Resistance Measurements Interposer Rev# 2
After presenting the first round of measurement data to the interposer supplier, changes were made to the TSV fabrication process and a second revision of interposer wafers were provided to test. The results of the second round of test data showed a huge improvement in the quality of the interposer. In version 1 of the interposers, out of the 28,475 test structures, there were approximately 276 failures. In the second version, for the same number of test structures the failures dropped to 9, a clear indication that process improvements/revisions could improve TSV yield.

TSV Vertical Connection Redundancy
In these experiments, the standard design of the interposer connections had a “one plus three” vertical redundant TSVs. It should also be noted that the same redundancy in revision one interposers did not prevent the failures. However, with the same redundancy, revision 2 interposers showed a much lower failure rate. While redundancy may hide a failure due to the multiple vertical parallel paths, the experiment could not determine the minimum amount of redundancy required.

Jung et al. [10] highlight the fact that adding redundant TSVs increases the size of the die and therefore, reduces the number of dies per wafer, increasing the cost of the die. They were also quick to point out through a mathematical model that if an interposer had 1E5 TSVs, the failure rate has to be no greater than 1E-7, to avoid redundant TSVs. This is well beyond today’s reality.

TSV Redundancy Vs Manufacturing Capability
Obtaining failure rates of 1E-7, while keeping the cost of manufacturing a TSV reasonable, seem to be at two ends of the spectrum. Therefore, the near-term solution is to add redundancy either in the form of two (or more) redundant vertical structures that form a parallel connection or as proposed previously [11], allocate six TSVs to a group for every four signals.

Production Testing of TSV's
Current production quality probe cards can probe structures 30 µm in diameter. Assuming that it at some point in the near future, it would be possible to probe a 10-µm TSV and ensure that it has good connectivity to the other side, 100 percent testing of TSVs would add significant cost to an interposer die. Until then, sample testing of dies will be the only way to create a wafer map of "presumed good interposer die." Secondly, the sole method currently available to test TSVs uses a daisy chain approach, consuming die real-estate and TSVs.
Additionally, to prevent 100% electrical test, the strategy for testing interposer would have be an "adaptive" approach where an algorithm such as the one used in the popular game "minesweeper" could be employed (Figure 15). If a failure were found in one die, then adjacent die should be tested; or if three surrounding dies have failures, it can be assumed that the die in the middle would fail too.

Figure 15: Adaptive test algorithms

Furthermore, within a wafer lot, the adaptive process should use die failure location information from previous wafers, and create a wafer map that identifies the most likely locations of failure in the wafer. The test program should test these dies and if failures are not found in the first several dies, the wafer confidence level increases, causing the test program to skip the next few likely fail die measurements.

Next Steps – Monitoring Quality
Daisy chain structures placed at die-corners can be used to extrapolate the quality of the interposer and generate a wafer map of "presumed good interposer die" (PGID). While most functional tests can verify the TSV continuity of the signal lines, redundancy in the case of power and ground may mask connectivity issues. One aspect of interposer testing can be to check the number of C4s that connects to a ground plane, or in a similar manner to a power plane. This could be achieved before die-attach if a dedicated metal layer on the front side of the interposer is reserved for a ground or power plane. If there are insufficient metal layers for each power plane, then a metal layer may be divided per plane.

To effectively test such structures, the probe card could be designed on a 20x20 grid which will be stepped across the interposer die. Those probe needles which make contact with the power or ground plane under test (PUT) will be activated. Of the possible 400 pin connections, pins that do not connect to the PUT will be disconnected by software commands. Each pin connected to the power plane will be individually energized by a small current of 100 µA, while the rest of the pins are connected to ground. The flow of current will indicate connectivity; furthermore, the measured voltage will indicate path resistance. This stepping pattern will be repeated until the desired pin coverage is achieved.

CURRENT TEST LIMITATIONS
With the given state of test technology today, and excluding the financial aspects, limitations have been identified.

One perceivable approach to 100% testing of an interposer wafer would be to provide a shorting block at the bottom of the interposer. This shorting block would short all the micro-bumps and the probe needles would push down on the C4 side. The challenge is the prober would have to handle 100-µm thickness wafers and with approximately 25,000 C4s and a probe needle BCF of 4 grams, a total force of 100 kilograms would be applied to the thinned wafer. Techniques need to be developed to handle this amount of force without potentially damage the interposer during test. Current probe needle technologies can probe bumps that are 25 µm to 30 µm in diameter, however, this technology cannot keep up with the continuous shrinking of micro-bump size.

CONCLUSION

While electrical test of interposers adds a level of confidence to the quality and connectivity of the die, it also adds cost and consumes real estate. Armed with test data, and mathematical models, we can conclude with high confidence that electrical testing of TSVs are not required after an interposer vendor is qualified and produces high-yielding wafers.

When the test step is eliminated, adding 100% automatic optical inspection (AOI) into the interposer fabrication process prevents blind-assembly builds. Furthermore, the AOI step acts as a process watchdog which can quickly identify excursions in manufacturing, sustain yields and provide high-quality interposers without test.

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